9-BIT PARITY GENERATOR AND CHECKER | 82S62

DIGITAL 8000 SERIES SCHOTTKY TTL/MSI

DESCRIPTION

The 82S62 9-Input Parity Generator/Parity Checker is a versatile MSI device commonly used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the 82S62. (A logic 1 on the INHIBIT input forces both outputs to a logic 0.)

When used as a Parity Generator, the 82S62 supplies a parity bit which is transmitted together with the data word.

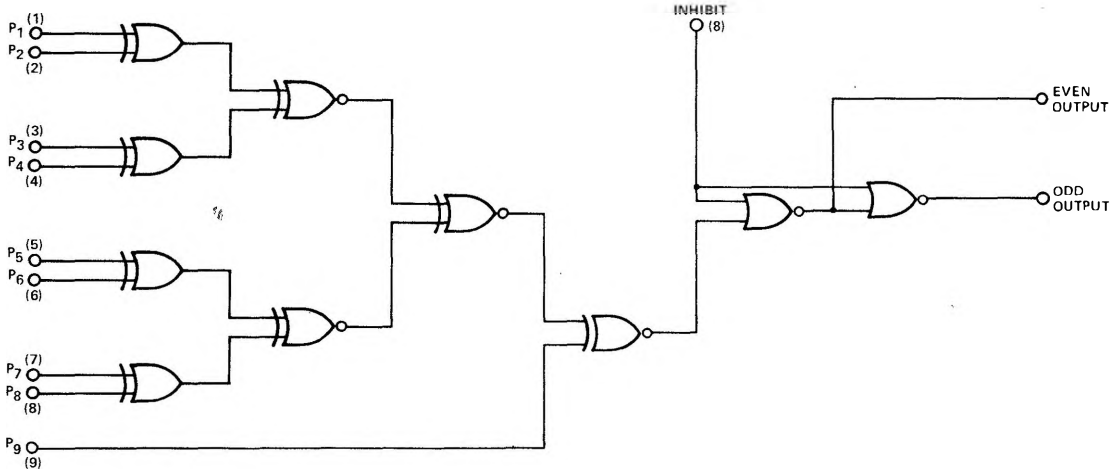
At the receiving end, the 82S62 acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- EVEN/ODD PARITY OUTPUTS
- INHIBIT INPUT
- PNP INPUTS

LOGIC DIAGRAM

82S62



V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers

LOGIC EQUATIONS:

Odd =

$\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$

Even =

$P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$

NOTE: Pin-Outs shown for Dual In-Line package only

ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature and Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN	TYP	MAX	UNITS	DATA INPUT UNDER TEST			
"1" Output Voltage								
Even	2.7			V	0V	.8V	–1mA	
Odd	2.7			V	2.0V	.8V	–1mA	
"0" Output Voltage								
Even			0.50	V	2.0V	.8V	20mA	
Odd			0.50	V	0V	.8V	20mA	
"0" Input Current								
Data Inputs P_1–P_8			–800	μA	0.5V			
Data Input P_9			–1.2	mA	0.5V			
Inhibit			–800	μA		0.5V		
"1" Input Current								
Data Inputs			10	μA	4.5V			
Inhibit			10	μA		4.5V		
Power/Current Consumption			355/67	mW/mA				11
Output Short Circuit Current	–40		–100					
Even	–40		–100	mA	0V	0V	0V	11
Odd	–40		–100	mA	4.0V	0V	0V	11

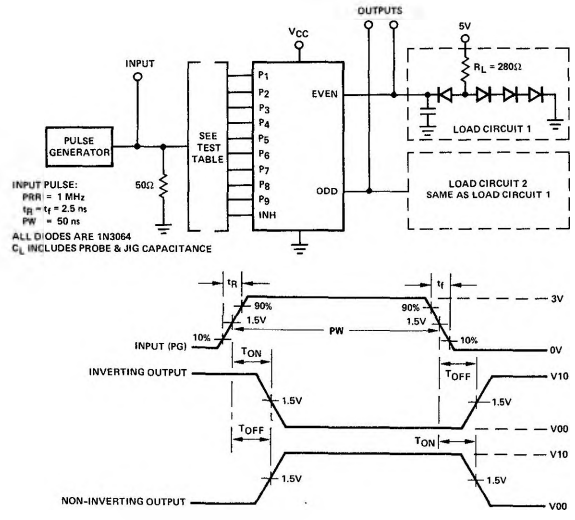
$T_A = 25^oC$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS	INHIBIT	OUTPUTS UNDER TEST	NOTES
	MIN	TYP	MAX	UNITS	UNDER TEST			
Turn-on/Turn-off Times								
P_1 – P_8 to Even			23	ns	Pulse			8
P_1 – P_8 to Odd			28	ns	Pulse			8
P_9 to Even			12	ns	Pulse			8
P_9 to Odd			18	ns	Pulse			8
Inhibit to Even			9	ns		Pulse		8
Inhibit to Odd			9	ns		Pulse		8

NOTES:

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. Manufacturer reserves the right to make design and process changes and improvements.
10. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
11. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS



TEST TABLE

TEST NO.	INPUTS P1	P2	P3	P4	P5	P6	P7	P8	P9	INH	OUTPUTS EVEN	ODD
1	PG	0	0	0	0	0	0	0	0	0		T
2	PG	0	0	0	0	0	0	0	0	0	T	T
3	0	0	PG	0	0	0	0	0	0	0	T	T
4	0	0	0	0	PG	0	0	0	0	0	T	T
5	0	0	0	0	0	0	PG	0	0	0	T	T
6	0	0	0	0	0	0	0	0	PG	0	T	T
7	0	0	0	0	0	0	0	0	0	PG	T	T

"1" = 2.7V "0" = GROUND

NOTE:

1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.