DESCRIPTION

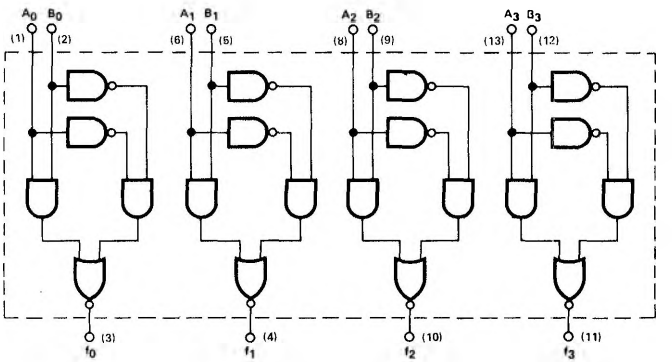
The 82S41 contains four independent gating structures to perform the Exclusive-OR function on two input variables. The output of the 82S41 employs the totem-pole structure characteristic of TTL devices.

FEATURES

- SCHOTTKY-CLAMPED TTL STRUCTURE
- PNP INPUTS

LOGIC DIAGRAMS

82S41 QUAD EXCLUSIVE–OR



A	B	f
0	0	0
1	0	1
0	1	1
1	1	0

V_{CC} = (14)
GND = (7)
( ) = Denotes Pin Numbers for 14-pin dual in-line package

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
					INPUTS		OUTPUTS	
	MIN.	TYP	MAX	UNITS	A	B		
Output "1" Voltage	2.7			V	2.0V	0.8V	−1mA	7
Output "0" Voltage			0.5	V	2.0V	2.0V	20mA	8
Input "1" Current			10	μA	4.5V	4.5V		11
Input "0" Current			−800	μA	0.5V	0.5V		12
Power/Current Consumption			290/55	mW/mA				13
Output Short Circuit Current	−40		−100	mA		−18mA	0V	13,10
Input Clamp Voltage	−1.2			V	−18mA			

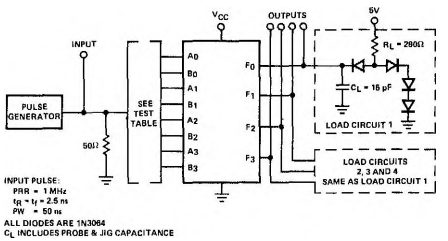
$T_A = 25^oC$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS			NOTES
					INPUTS		OUTPUTS	
	MIN	TYP	MAX	UNITS	A	B		
Turn-On/Turn-Off Times			10	ns				9

NOTES:

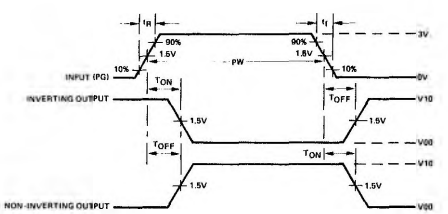
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive NAND logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Measurements apply to each gate element independently.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_{CC}.
9. Refer to AC Test Figure.
10. Not more than one output should be shorted at a time.
11. A and B are tested separately. When A is 4.5V, B is 0V, and vice versa.
12. A and B are tested separately. When A is 0.4V, B is 5.25V, and vice versa.
13. V_{CC} = 5.25V.

AC TEST FIGURE AND WAVEFORMS



TEST TABLE												
TEST NO.	INPUTS								OUTPUTS			
	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3
1	0	0	0	PG	0	0	0	0		T		
2	0	PG	0	0	0	0	0	0	T			
3	0	0	0	PG	0	0	0	0		T		
4	0	0	0	0	0	PG	0	0			T	
5	0	0	0	0	0	0	0	PG				T
6	PG	0	0	0	0	0	0	0	T			
7	0	0	0	0	0	0	PG	0				T

"1" = 2.7V "0" = GROUND



NOTE:

1. A.C. TEST JIGS MUST NOT HAVE ANY SWITCHES.
2. A.C. TEST JIGS MUST HAVE LESS THAN 1/8 INCH LEAD LENGTH FROM PACKAGE PINS.