OBJECTIVE SPECIFICATION

82S400/400A - I • 82S401/401A - I

DESCRIPTION

The 82S400 and 82S401, with typical access time of 45ns, are ideal for cache buffer applications and for systems requiring very high speed main memory. The 82S400A and 82S401A are devices selected for speed compatibility with industry standard 1024-bit RAMs having 45ns access time.

Both devices require a single +5V power supply, feature very low current pnp input structures, and include on-chip decoding and a chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

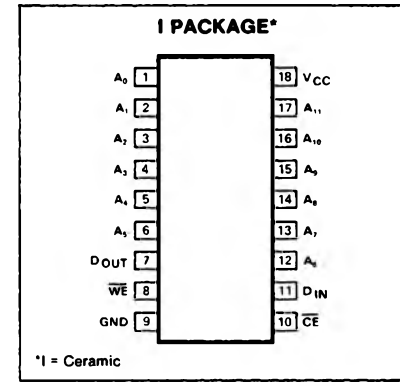
APPLICATIONS

- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

FEATURES

- **Address access time:**
  82S400/401: 70ns max
  82S400A/401A: 45ns max
- **Write cycle time: 70ns max**
- **Power dissipation: 0.12mW/bit typ**
- **Input loading: -150μA max**
- **On-chip address decoding**
- **Output options:**
  82S400: Open collector
  82S401: Tri-state
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

PIN CONFIGURATION



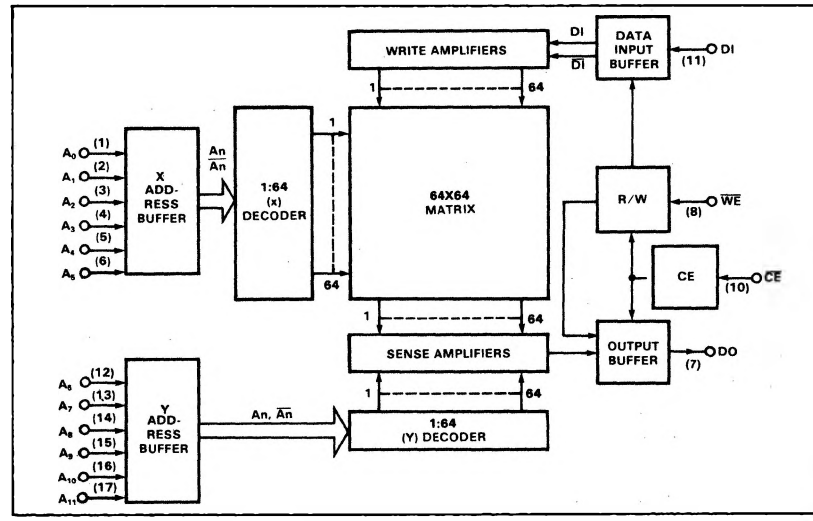
*I = Ceramic

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}	
				82S400	82S401
Read	0	1	X	Stored data	Stored data
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S400)	+5.5	
V_O	Off-state (82S401)	+5.5	
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
	Input voltage					V
V_{IL}	Low[1]	V_{CC} = Min			.85	
V_{IH}	High[1]	V_{CC} = Max	2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -12mA		-1.0	-1.5	
	Output voltage	V_{CC} = Min				V
V_{OL}	Low[1,4]	I_{OL} = 16mA		0.35	0.45	
V_{OH}	High (82S401)[1,5]	I_{OH} = -2mA	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V		-25	-150	
I_{IH}	High	V_{IN} = 5.5V		1	25	
	Output current	V_{CC} = Max				
I_{OLK}	Leakage (82S400)[6]	V_{OUT} = 5.5V		1	40	μA
$I_{O(OFF)}$	Hi-Z state (82S401)[6]	V_{OUT} = 5.5V		1	60	μA
		V_{OUT} = 0.45V		-1	-60	
I_{OS}	Short circuit (82S401)[7]	V_{OUT} = 0V	-20		-100	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max				mA
		$0 < T_A < 25°C$		120	155	
		$T_A \ge 25°C$		105	130	
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		4		
C_{OUT}	Output	V_{OUT} = 2.0V		7		

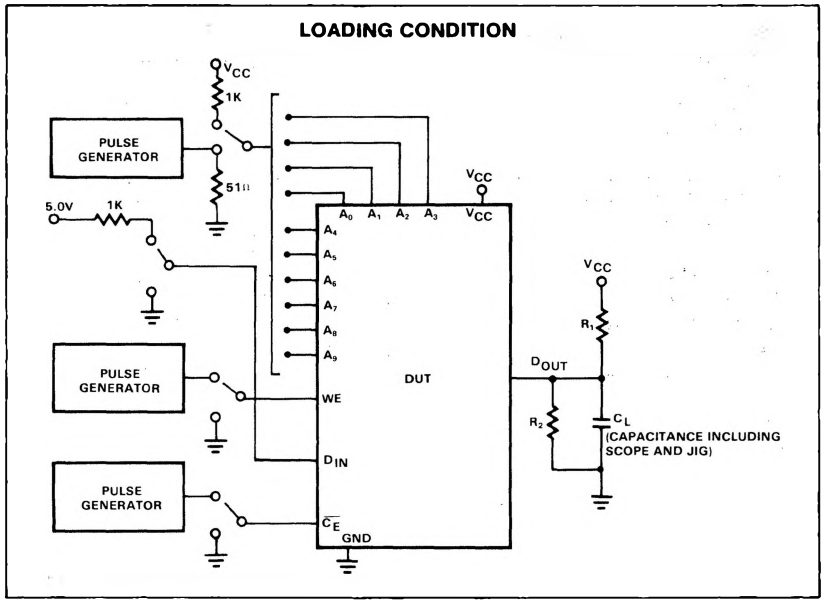
AC ELECTRICAL CHARACTERISTICS $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$, $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$

PARAMETER		TO	FROM	N82S400A/401A			N82S400/401			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{AA}		Output	Address			45		45	70	
T_{CE}		Output	Chip enable			30		30	45	
	Disable time									ns
T_{CD}		Output	Chip enable			30		30	45	
T_{WD}		Output	Write enable			30		30	45	
T_{WR}	Recovery time	Output	Write enable			30		30	45	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	5			10	5		
T_{WHA}	Hold time									
T_{WSD}	Setup time	Write enable	Data in	35			50	35		
T_{WHD}	Hold time			5			10	5		
T_{WSC}	Setup time	Write enable	CE	5			10	5		
T_{WHC}	Hold time									
	Pulse width[9]									ns
T_{WP}	Write enable			35			50	35		

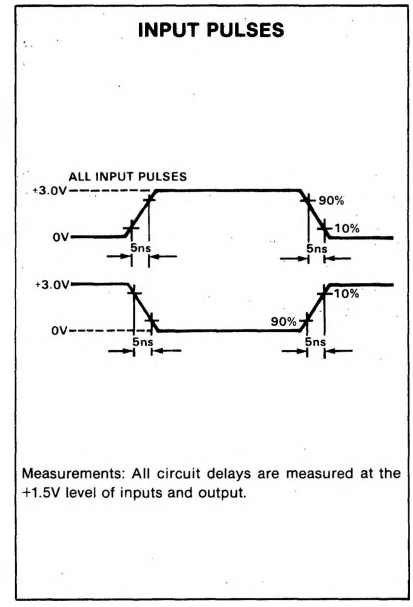
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A 25°C.
3. Test each input one at a time.
4. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
    Θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
    Θ_{JA} junction to ambient - still air - 90°C/watt
    Θ_{JA} junction to case - 20°C/watt

TEST LOAD CIRCUIT

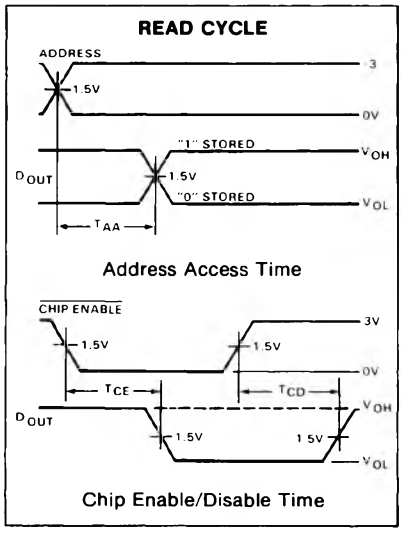


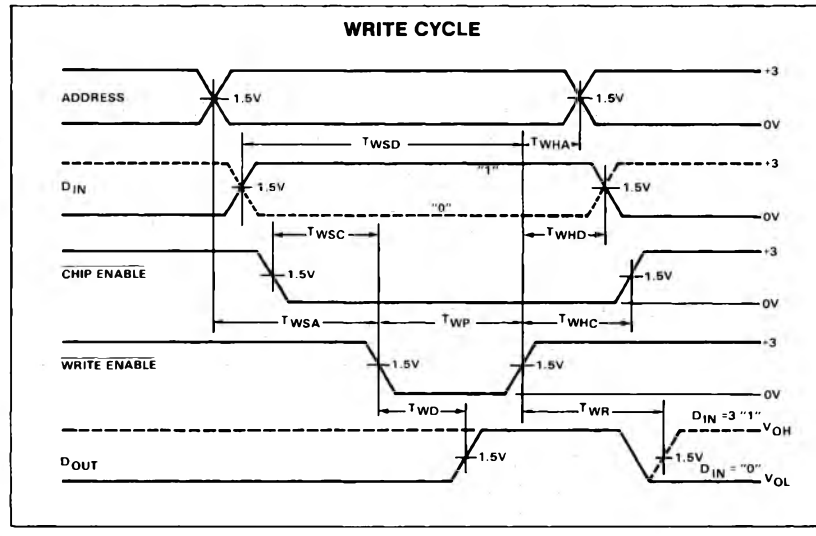
VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and output.

TIMING DIAGRAMS





TIMING DEFINITIONS

T_{WR} Delay between end of Write Enable pulse and when Data Output becomes valid (assuming Address still valid—not as shown).

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state.

T_{AA} Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.

T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.

T_{WHD} Required delay between end of Write Enable pulse and end of valid Input Data.

T_{WP} Width of Write Enable pulse.

T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.

T_{WSD} Required delay between beginning of valid Data Input and end of Write Enable pulse.

T_{WD} Delay between beginning of Write Enable pulse and when Data Output is in off state.

T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.

T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.