



- A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in micro-computer systems.

FUNCTIONAL DESCRIPTION

Microprocessors like the 8080 are MOS devices and are generally capable of driving a single TTL load. The same is true for MOS memory devices. While this type of drive is sufficient in small systems with few components, quite often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The 8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

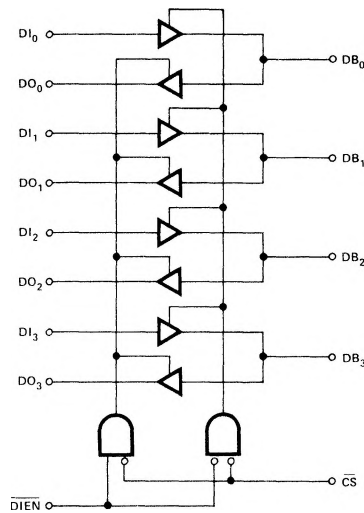
Each buffered line of the four bit driver consists of two separate buffers that are tri-state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is direct TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080 Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080 and 8008 CPUs is achieved with an adequate amount of noise immunity (350mV worst case).

Control Gating $\overline{\text{DIEN}}$, $\overline{\text{CS}}$

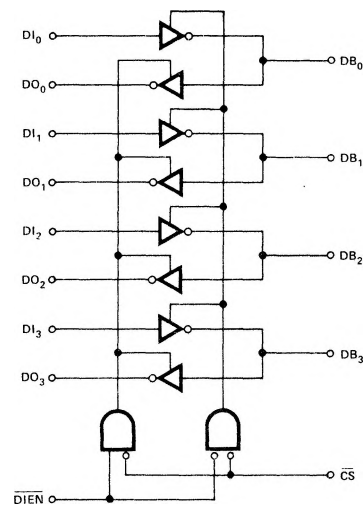
The $\overline{\text{CS}}$ input is actually a device select. When it is "high" the output drivers are all forced to their high-impedance state. When it is at "zero" the device is selected (enabled) and the direction of the data flow is determined by the $\overline{\text{DIEN}}$ input.

The $\overline{\text{DIEN}}$ input controls the direction of data flow (see Figure 1) for complete truth table. This direction control is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

The 8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.



(a) 8216



(b) 8226

DIEN	CS	
0	0	DI · DB
1	0	DB · DO
0	1	HIGH IMPEDANCE
1	1	

Figure 1. 8216/8226 Logic Diagrams

APPLICATIONS OF 8216/8226

8080 Data Bus Buffer

The 8080 CPU Data Bus is capable of driving a single TTL load and is more than adequate for small, single board systems. When expanding such a system to more than one board to increase I/O or Memory size, it is necessary to provide a buffer. The 8216/8226 is a device that is exactly fitted to this application.

Shown in Figure 2 are a pair of 8216/8226 connected directly to the 8080 Data Bus and associated control signals. The buffer is bi-directional in nature and serves to isolate the CPU data bus.

On the system side, the DB lines interface with standard semiconductor I/O and Memory components and are completely TTL compatible. The DB lines also provide a high drive capability (50mA) so that an extremely large system can be driven along with possible bus termination networks.

On the 8080 side the DI and DO lines are tied together and are directly connected to the 8080 Data Bus for bi-directional operation. The DO outputs of the 8216/8226 have a high voltage output capability of 3.65 volts which allows direct connection to the 8080 whose minimum input voltage is 3.3 volts. It also gives a very adequate noise margin of 350mV (worst case).

The $\overline{\text{DIEN}}$ inputs to 8216/8226 is connected directly to the 8080. $\overline{\text{DIEN}}$ is tied to $\overline{\text{DBIN}}$ so that proper bus flow is maintained, and CS is tied to $\overline{\text{BUSEN}}$ so that the system side Data Bus will be 3-stated when a Hold request has been acknowledged during a DMA activity.

Memory and I/O Interface to a Bi-directional Bus

In large microcomputer systems it is often necessary to provide Memory and I/O with their own buffers and at the same time maintain a direct, common interface to a bi-directional Data Bus. The 8216/8226 has separated data in and data out lines on one side and a common bi-directional set on the other to accommodate such a function.

Shown in Figure 3 is an example of how the 8216/8226 is used in this type of application.

The interface to Memory is simple and direct. The memories used are typically Intel[®] 8102, 8102A, 8101 or 8107B-4 and have separate data inputs and outputs. The DI and DO lines of the 8216/8226 tie to them directly and under control of the $\overline{\text{MEMR}}$ signal, which is connected to the $\overline{\text{DIEN}}$ input, an interface to the bi-directional Data Bus is maintained.

The interface to I/O is similar to Memory. The I/O devices used are typically Intel[®] 8255s, and can be used for both input and output ports. The I/O R signal is connected directly to the $\overline{\text{DIEN}}$ input so that proper data flow from the I/O device to the Data Bus is maintained.

The 8216/8226 can be used in a wide variety of other buffering functions in microcomputer systems such as Address Bus Drivers, Drivers to peripheral devices such as printers, and as Drivers for long length cables to other peripherals or systems.

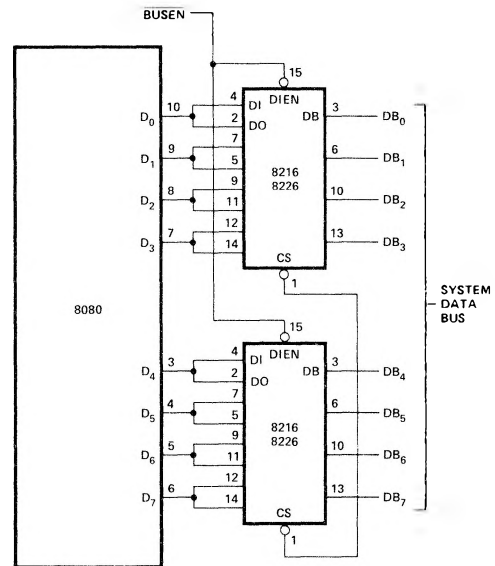


Figure 2. 8080 Data Bus Buffer.

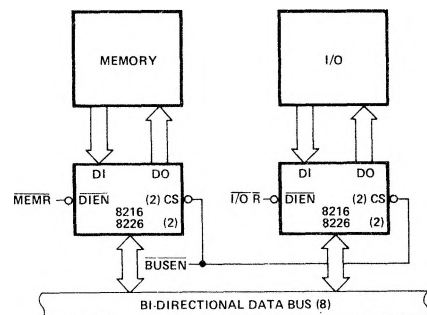


Figure 3. Memory and I/O Interface to a Bi-Directional Bus.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
All Output and Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to +5.5V
Output Currents	125 mA

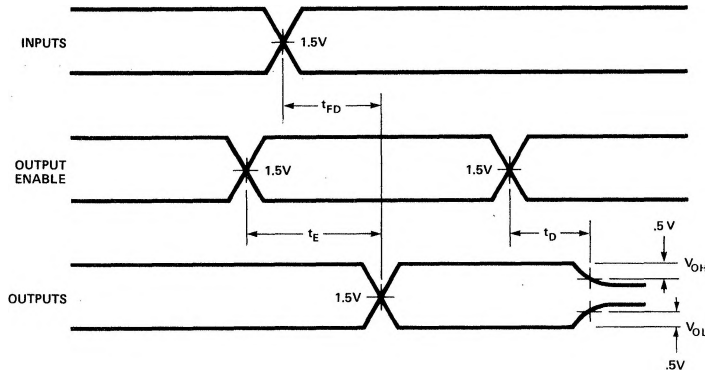
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.	Max.		
I_{F1}	Input Load Current DIEN, CS		-0.15	-.5	mA	$V_F = 0.45$
I_{F2}	Input Load Current All Other Inputs		-0.08	-.25	mA	$V_F = 0.45$
I_{R1}	Input Leakage Current DIEN, CS			20	μA	$V_R = 5.25V$
I_{R2}	Input Leakage Current DI Inputs			10	μA	$V_R = 5.25V$
V_C	Input Forward Voltage Clamp			-1	V	$I_C = -5\text{mA}$
V_{IL}	Input "Low" Voltage			.95	V	
V_{IH}	Input "High" Voltage	2.0			V	
$ I_{OL} $	Output Leakage Current (3-State) DO DB			20 100	μA	$V_O = 0.45V/5.25V$
I_{CC}	Power Supply Current 8216		95	130	mA	
	8226		85	120	mA	
V_{OL1}	Output "Low" Voltage		0.3	.45	V	DO Outputs $I_{OL} = 15\text{mA}$ DB Outputs $I_{OL} = 25\text{mA}$
V_{OL2}	Output "Low" Voltage 8216		0.5	.6	V	DB Outputs $I_{OL} = 55\text{mA}$
	8226		0.5	.6	V	DB Outputs $I_{OL} = 50\text{mA}$
V_{OH1}	Output "High" Voltage	3.65	4.0		V	DO Outputs $I_{OH} = -1\text{mA}$
V_{OH2}	Output "High" Voltage	2.4	3.0		V	DB Outputs $I_{OH} = -10\text{mA}$
I_{OS}	Output Short Circuit Current	-15	-35	-65	mA	DO Outputs $V_O \cong 0V$,
		-30	-75	-120	mA	DB Outputs $V_{CC} = 5.0V$

NOTE: Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0V$.

WAVEFORMS



A.C. CHARACTERISTICS

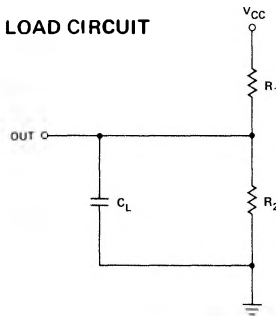
$T_A = 0^\circ\text{C to } +70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[1]	Max.		
T_{PD1}	Input to Output Delay DO Outputs		15	25	ns	$C_L = 30\text{pF}$, $R_1 = 300\Omega$ $R_2 = 600\Omega$
T_{PD2}	Input to Output Delay DB Outputs		20	30	ns	$C_L = 300\text{pF}$, $R_1 = 90\Omega$
			16	25	ns	$R_2 = 180\Omega$
T_E	Output Enable Time		45	65	ns	(Note 2)
			35	54	ns	(Note 3)
T_D	Output Disable Time		20	35	ns	(Note 4)

TEST CONDITIONS:

Input pulse amplitude of 2.5V.
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

TEST LOAD CIRCUIT



CAPACITANCE [5]

Symbol	Parameter	Limits			Unit
		Min.	Typ.[1]	Max.	
C_{IN}	Input Capacitance		4	8	pF
C_{OUT1}	Output Capacitance		6	10	pF
C_{OUT2}	Output Capacitance		13	18	pF

TEST CONDITIONS: $V_{BIAS} = 2.5\text{V}$, $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$.

- NOTES:
- Typical values are for $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$.
 - DO Outputs, $C_L = 30\text{pF}$, $R_1 = 300/10\text{ K}\Omega$, $R_2 = 180/1\text{ K}\Omega$; DB Outputs, $C_L = 300\text{pF}$, $R_1 = 90/10\text{ K}\Omega$, $R_2 = 180/1\text{ K}\Omega$.
 - DO Outputs, $C_L = 30\text{pF}$, $R_1 = 300/10\text{ K}\Omega$, $R_2 = 600/1\text{ K}\Omega$; DB Outputs, $C_L = 300\text{pF}$, $R_1 = 90/10\text{ K}\Omega$, $R_2 = 180/1\text{ K}\Omega$.
 - DO Outputs, $C_L = 5\text{pF}$, $R_1 = 300/10\text{ K}\Omega$, $R_2 = 600/1\text{ K}\Omega$; DB Outputs, $C_L = 5\text{pF}$, $R_1 = 90/10\text{ K}\Omega$, $R_2 = 180/1\text{ K}\Omega$.
 - This parameter is periodically sampled and not 100% tested.