

# 54F251A,74F251A

*54F251A 74F251A 8-Input Multiplexer with TRI-STATE Outputs*



Literature Number: SNOS178A

# 54F/74F251A 8-Input Multiplexer with TRI-STATE® Outputs

## General Description

The 74F251A is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

## Features

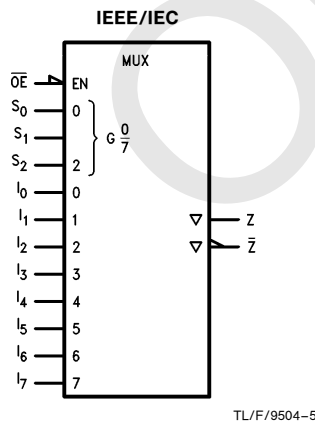
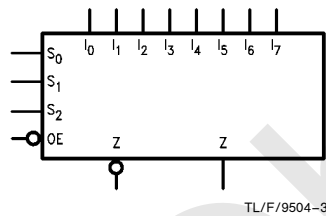
- Multifunctional capability
- On-chip select logic decoding
- Inverting and non-inverting TRI-STATE outputs

Commercial	Military	Package Number	Package Description
74F251APC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F251ADM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F251ASC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F251ASJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F251AFM (Note 2)	W16A	16-Lead Cerpack
	54F251ALL (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

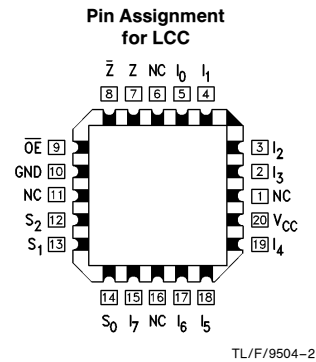
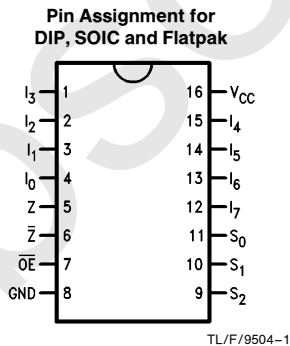
**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

## Logic Symbols



## Connection Diagrams



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$S_0-S_2$	Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I_0-I_7$	Multiplexer Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
Z	TRI-STATE Multiplexer Output	150/40 (33.3)	-3 mA/24 mA (20 mA)
$\overline{Z}$	Complementary TRI-STATE Multiplexer Output	150/40 (33.3)	-3 mA/24 mA (20 mA)

## Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0$ ,  $S_1$ ,  $S_2$ . Both assertion and negation outputs are provided. The Output Enable input ( $\overline{OE}$ ) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

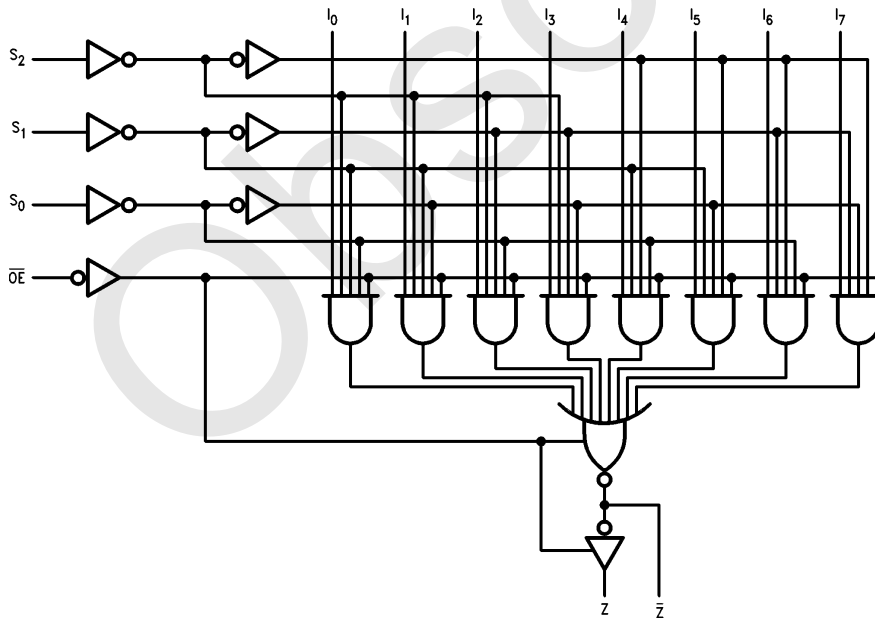
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

## Truth Table

$\overline{OE}$	Inputs			Outputs	
	$S_2$	$S_1$	$S_0$	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I_0}$	$I_0$
L	L	L	H	$\overline{I_1}$	$I_1$
L	L	H	L	$\overline{I_2}$	$I_2$
L	L	H	H	$\overline{I_3}$	$I_3$
L	H	L	L	$\overline{I_4}$	$I_4$
L	H	L	H	$\overline{I_5}$	$I_5$
L	H	H	L	$\overline{I_6}$	$I_6$
L	H	H	H	$\overline{I_7}$	$I_7$

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

## Logic Diagram



TL/F/9504-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I<sub>OL</sub> (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

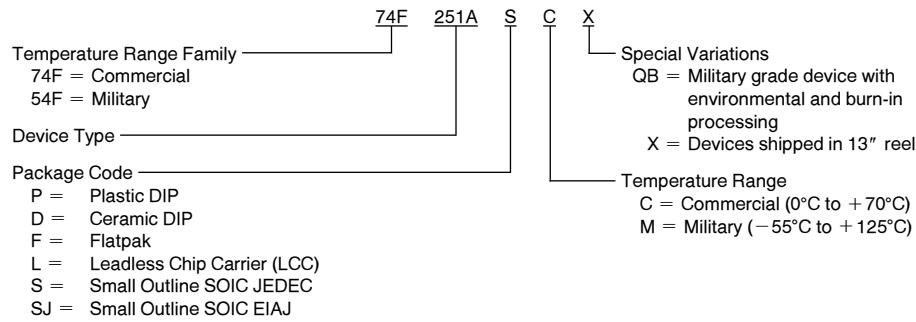
Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA
		54F 10% V <sub>CC</sub>	2.4				
		74F 10% V <sub>CC</sub>	2.5				
		74F 10% V <sub>CC</sub>	2.4				
		74F 5% V <sub>CC</sub>	2.7				
		74F 5% V <sub>CC</sub>	2.7				
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
		74F 10% V <sub>CC</sub>		0.5			
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current			-60	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCL</sub>	Power Supply Current		15	22	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		16	24	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics

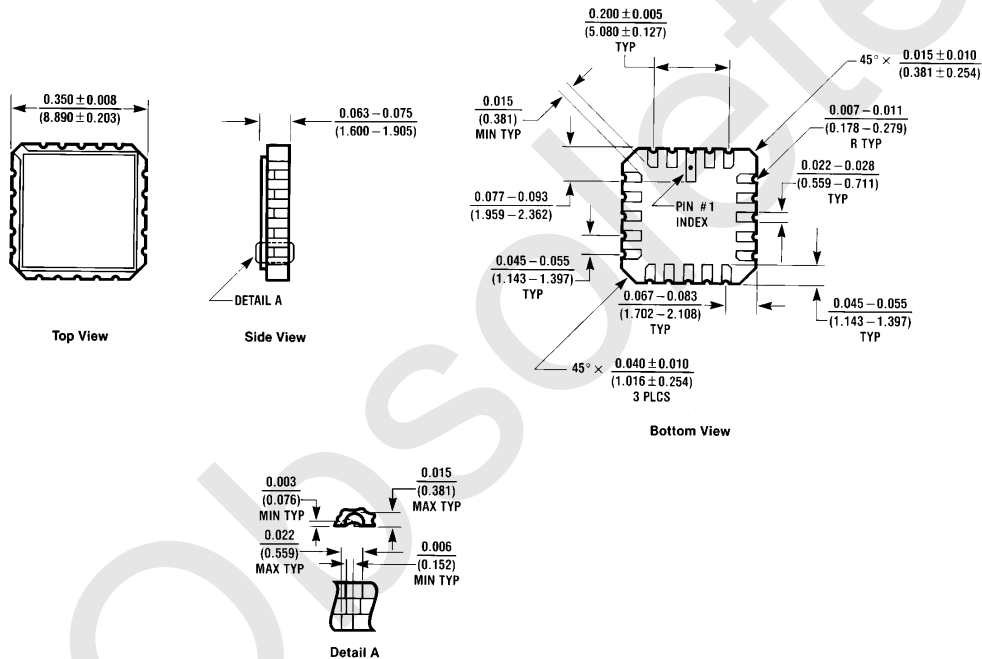
Symbol	Parameter	74F			54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to $\bar{Z}$	3.5 3.2	6.0 5.0	9.0 7.5	3.5 3.2	11.5 8.0	3.5 3.2	9.5 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to Z	4.5 4.0	7.5 6.0	10.5 8.5	3.5 3.0	14.0 10.5	4.5 4.0	12.5 9.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to $\bar{Z}$	3.0 1.5	5.0 2.5	6.5 4.0	2.5 1.5	8.0 6.0	3.0 1.5	7.0 5.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z	3.5 3.5	5.0 5.5	7.0 7.0	2.5 3.5	9.0 9.0	2.5 3.5	8.0 7.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\bar{OE}$ to $\bar{Z}$	2.5 2.5	4.3 4.3	6.0 6.0	2.0 2.5	7.0 7.5	2.5 2.5	7.0 6.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\bar{OE}$ to $\bar{Z}$	2.5 1.5	4.0 3.0	5.5 4.5	2.5 1.5	6.0 5.0	2.5 1.5	6.0 4.5	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\bar{OE}$ to Z	3.5 3.5	5.0 5.5	7.0 7.5	3.0 3.5	8.5 9.0	3.0 3.5	7.5 8.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\bar{OE}$ to Z	2.0 1.5	3.8 3.0	5.5 4.5	2.0 1.5	5.5 5.5	2.0 1.5	5.5 4.5	

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



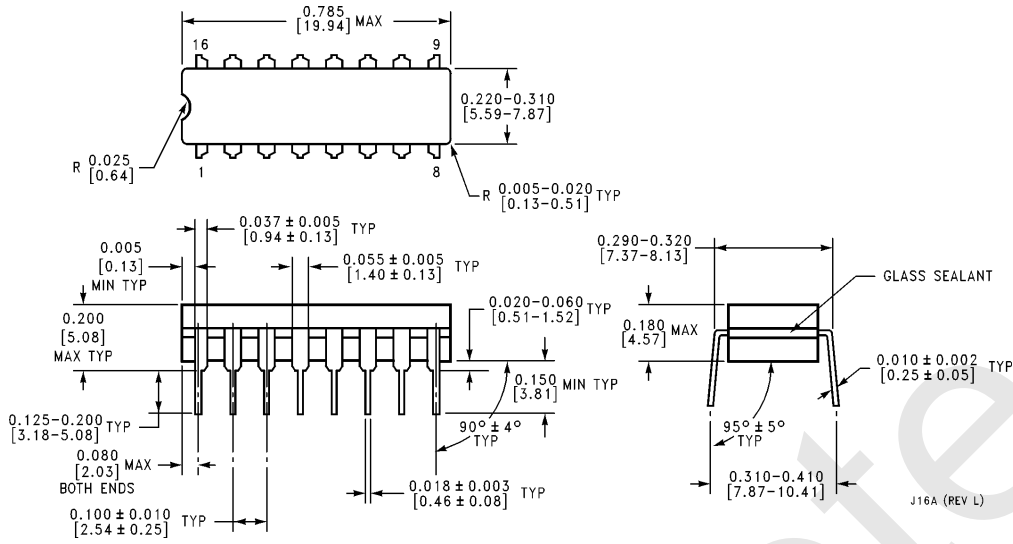
## Physical Dimensions inches (millimeters)



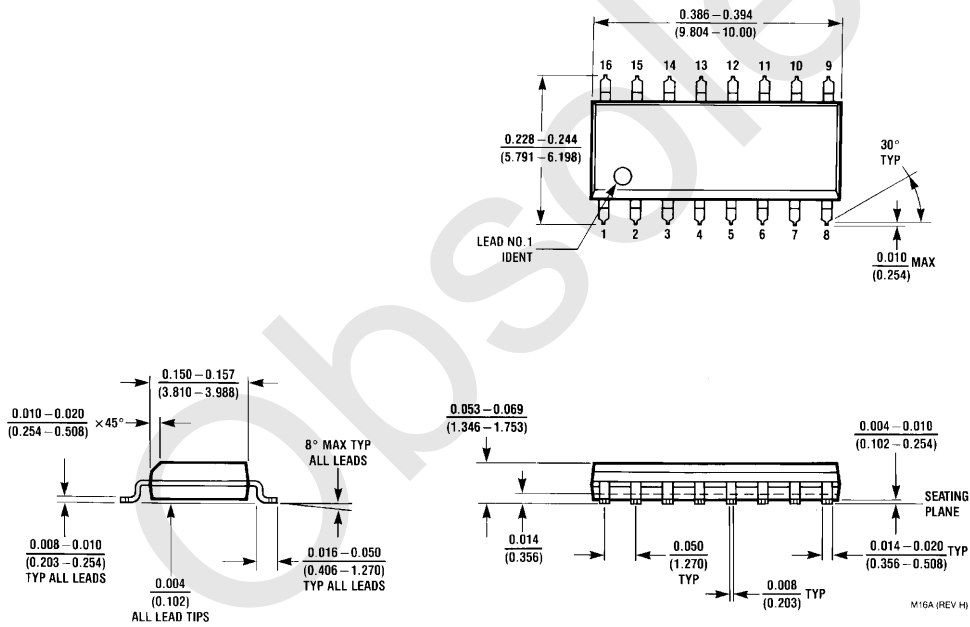
**20-Lead Ceramic Leadless Chip Carrier (L)  
NS Package Number E20A**

E20A (REV D)

**Physical Dimensions** inches (millimeters) (Continued)

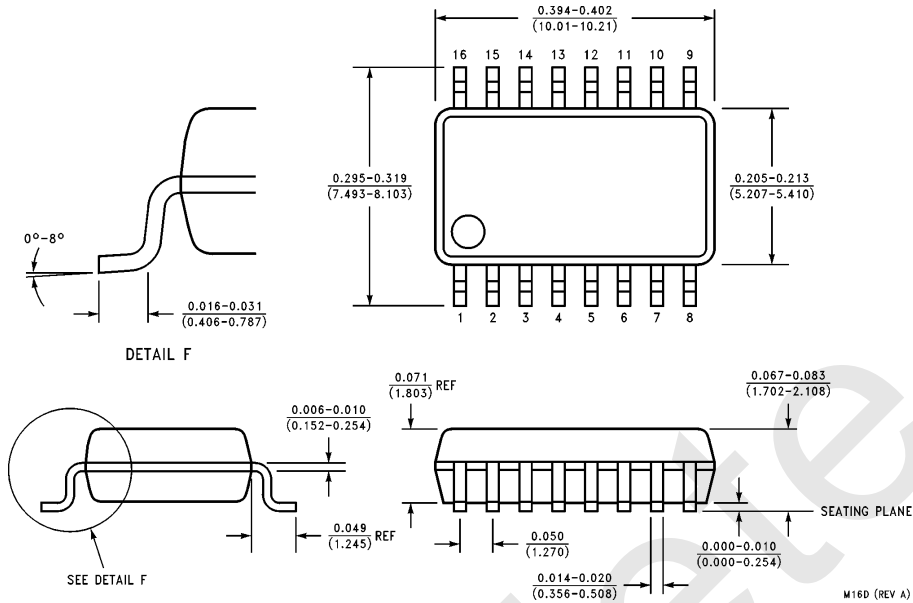


**16-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J16A

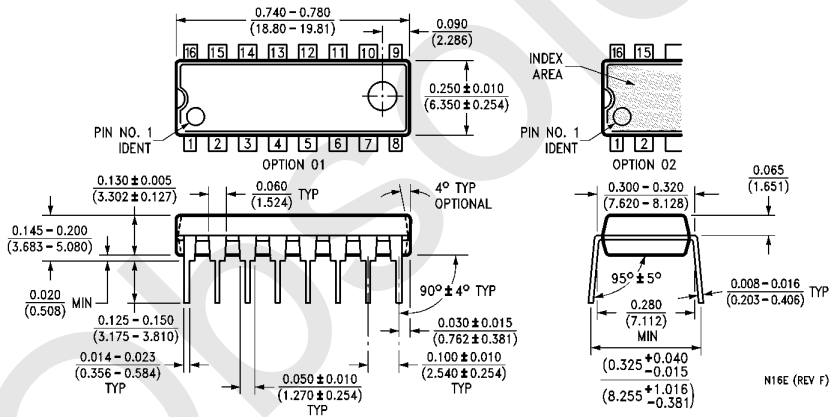


**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)**  
NS Package Number M16A

**Physical Dimensions** inches (millimeters) (Continued)



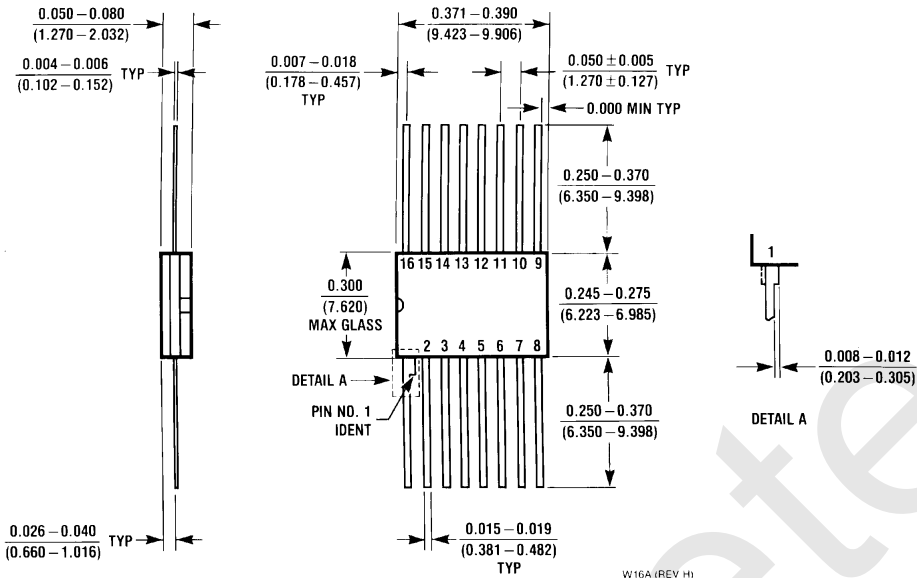
**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)  
NS Package Number M16D**



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)  
NS Package Number N16E**



**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead Ceramic Flatpak (F)  
NS Package Number W16A**

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