

# DATA SHEET

## **74AHC1G00; 74AHCT1G00** 2-input NAND gate

Product specification  
Supersedes data of 1998 Nov 25  
File under Integrated Circuits, IC06

1999 Jan 27

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## FEATURES

- Symmetrical output impedance
- High noise immunity
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V
- Low power dissipation
- Balanced propagation delays
- Very small 5-pin package
- Output capability: standard.

## DESCRIPTION

The 74AHC1G/AHCT1G00 is a high-speed Si-gate CMOS device.

The 74AHC1G/AHCT1G00 provides the 2-input NAND function.

## FUNCTION TABLE

See note 1.

INPUTS		OUTPUT
inA	inB	outY
L	L	H
L	H	H
H	L	H
H	H	L

## Note

1. H = HIGH voltage level.  
L = LOW voltage level.

## ORDERING AND PACKAGE INFORMATION

TYPE NUMBER	PACKAGES					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74AHC1G00GW	-40 to +85 °C	5	SC-88A	plastic	SOT353	AA
74AHCT1G00GW		5	SC-88A	plastic	SOT353	CA

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ °C}$ ;  $t_r = t_f \leq 3.0\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			AHC1G	AHCT1G	
$t_{PHL}/t_{PLH}$	propagation delay inA, inB to outY	$C_L = 15\text{ pF}$ $V_{CC} = 5\text{ V}$	3.5	3.6	ns
$C_I$	input capacitance		1.5	1.5	pF
$C_{PD}$	power dissipation capacitance	notes 1 and 2; $C_L = 50\text{ pF}$ ; $f = 1\text{ MHz}$	17	18	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in V.
2. The condition is  $V_I = \text{GND}$  to  $V_{CC}$ .

## PINNING

PIN	SYMBOL	DESCRIPTION
1	inB	data input
2	inA	data input
3	GND	ground (0 V)
4	outY	data output
5	$V_{CC}$	DC supply voltage

# 2-input NAND gate

# 74AHC1G00; 74AHCT1G00

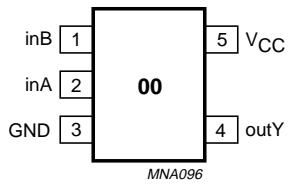


Fig.1 Pin configuration.

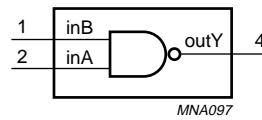


Fig.2 Logic symbol.



Fig.3 IEC logic symbol.

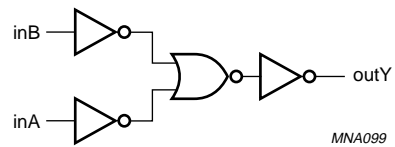


Fig.4 Logic diagram.

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC1G			74AHCT1G			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	DC supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	–	5.5	0	–	5.5	V
$V_O$	output voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature range	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
$t_r, t_f (\Delta t/\Delta f)$	input rise and fall times except for Schmitt-trigger inputs	$V_{CC} = 3.3 V \pm 0.3 V$	–	–	100	–	–	–	ns/V
		$V_{CC} = 5 V \pm 0.5 V$	–	–	20	–	–	20	

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	DC supply voltage		–0.5	+7.0	V
$V_I$	input voltage range		–0.5	+7.0	V
$I_{IK}$	DC input diode current	$V_I < -0.5$	–	–20	mA
$I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5 V$ ; note 1	–	$\pm 20$	mA
$I_O$	DC output source or sink current	$-0.5 V < V_O < V_{CC} + 0.5 V$	–	$\pm 25$	mA
$I_{CC}$	DC $V_{CC}$ or GND current		–	$\pm 75$	mA
$T_{stg}$	storage temperature range		–65	+150	°C
$P_D$	power dissipation per package	temperature range: –40 to +85 °C; note 2	–	200	mW

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above +55 °C the value of  $P_D$  derates linearly with 2.5 mW/K.

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## DC CHARACTERISTICS

## Family 74AHC1G

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)					UNIT
		OTHER	V <sub>CC</sub> (V)	+25			-40 to +85		
				MIN.	TYP.	MAX.	MIN.	MAX.	
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	
			5.5	3.85	–	–	3.85	–	
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	
			5.5	–	–	1.65	–	1.65	
V <sub>OH</sub>	HIGH-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –50 µA	2.0	1.9	2.0	–	1.9	–	V
			3.0	2.9	3.0	–	2.9	–	
			4.5	4.4	4.5	–	4.4	–	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –4.0 mA	3.0	2.58	–	–	2.48	–	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –8.0 mA	4.5	3.94	–	–	3.8	–	
V <sub>OL</sub>	LOW-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 50 µA	2.0	–	0	0.1	–	0.1	V
			3.0	–	0	0.1	–	0.1	
			4.5	–	0	0.1	–	0.1	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4 mA	3.0	–	–	0.36	–	0.44	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8 mA	4.5	–	–	0.36	–	0.44	
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	0.1	–	1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	1.0	–	10	µA
C <sub>I</sub>	input capacitance			–	1.5	10	–	10	pF

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

**Family 74AHCT1G**

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)					UNIT
		OTHER	V <sub>CC</sub> (V)	+25			-40 to +85		
				MIN.	TYP.	MAX.	MIN.	MAX.	
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	2.0	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –50 µA	4.5	4.4	4.5	–	4.4	–	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –8.0 mA	4.5	3.94	–	–	3.8	–	V
V <sub>OL</sub>	LOW-level output voltage; all outputs	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 50 µA	4.5	–	0	0.1	–	0.1	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 8 mA	4.5	–	–	0.36	–	0.44	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	5.5	–	–	0.1	–	1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	1.0	–	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = 3.4 V other inputs at V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	1.35	–	1.5	mA
C <sub>I</sub>	input capacitance			–	1.5	10	–	10	pF

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## AC CHARACTERISTICS

## Type 74AHC1G00

GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS			T <sub>amb</sub> (°C)					UNIT
		WAVEFORMS	C <sub>L</sub>	V <sub>CC</sub> (V)	+25			-40 to +85		
					MIN.	TYP.	MAX.	MIN.	MAX.	
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay inA, inB to outY	see Figs 5 and 6	15 pF	3.0 to 3.6	–	4.5 <sup>(1)</sup>	7.9	1.0	9.5	ns
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay inA, inB to outY	see Figs 5 and 6	50 pF	3.0 to 3.6	–	6.5 <sup>(1)</sup>	11.4	1.0	13.0	ns
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay inA, inB to outY	see Figs 5 and 6	15 pF	4.5 to 5.5	–	3.5 <sup>(2)</sup>	5.5	1.0	6.5	ns
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay inA, inB to outY	see Figs 5 and 6	50 pF	4.5 to 5.5	–	4.9 <sup>(2)</sup>	7.5	1.0	8.5	ns

## Notes

1. Typical values at V<sub>CC</sub> = 3.3 V.
2. Typical values at V<sub>CC</sub> = 5.0 V.

## Type 74AHCT1G00

GND = 0 V;  $t_r = t_f \leq 3.0$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS			T <sub>amb</sub> (°C)					UNIT
		WAVEFORMS	C <sub>L</sub>	V <sub>CC</sub> (V)	+25			-40 to +85		
					MIN.	TYP.	MAX.	MIN.	MAX.	
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay inA, inB to outY	see Figs 5 and 6	15 pF	4.5 to 5.5	–	3.6 <sup>(1)</sup>	6.9	1.0	8.0	ns
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay inA, inB to outY	see Figs 5 and 6	50 pF	4.5 to 5.5	–	5.0 <sup>(1)</sup>	7.9	1.0	9.0	ns

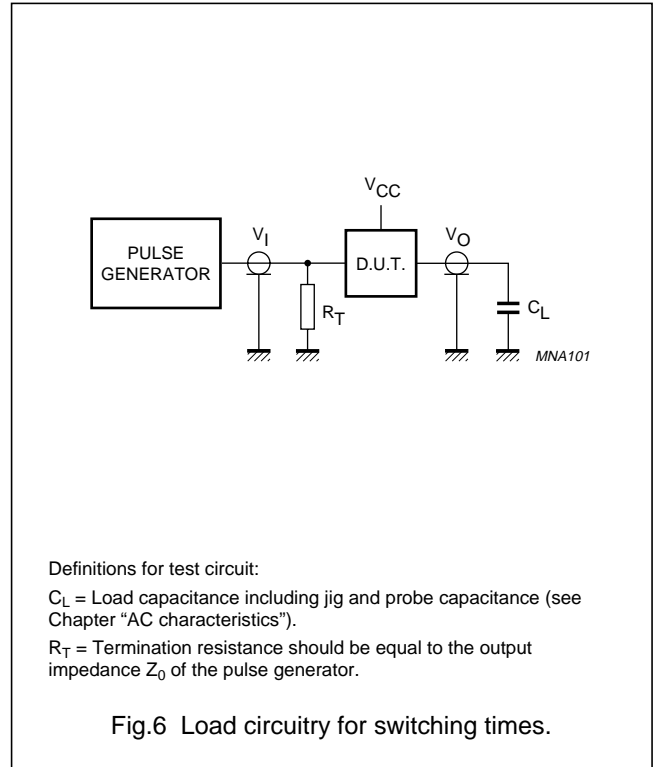
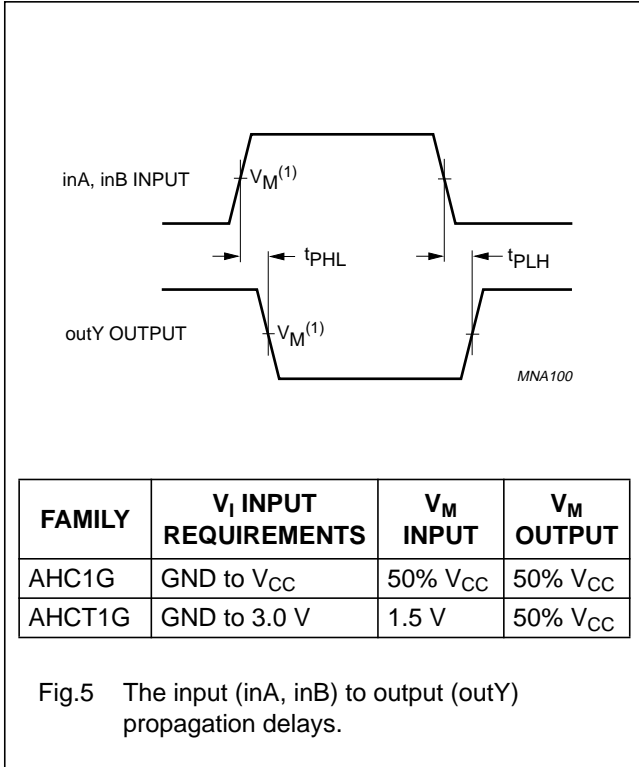
## Note

1. Typical values at V<sub>CC</sub> = 5.0 V.

2-input NAND gate

74AHC1G00; 74AHCT1G00

AC WAVEFORMS





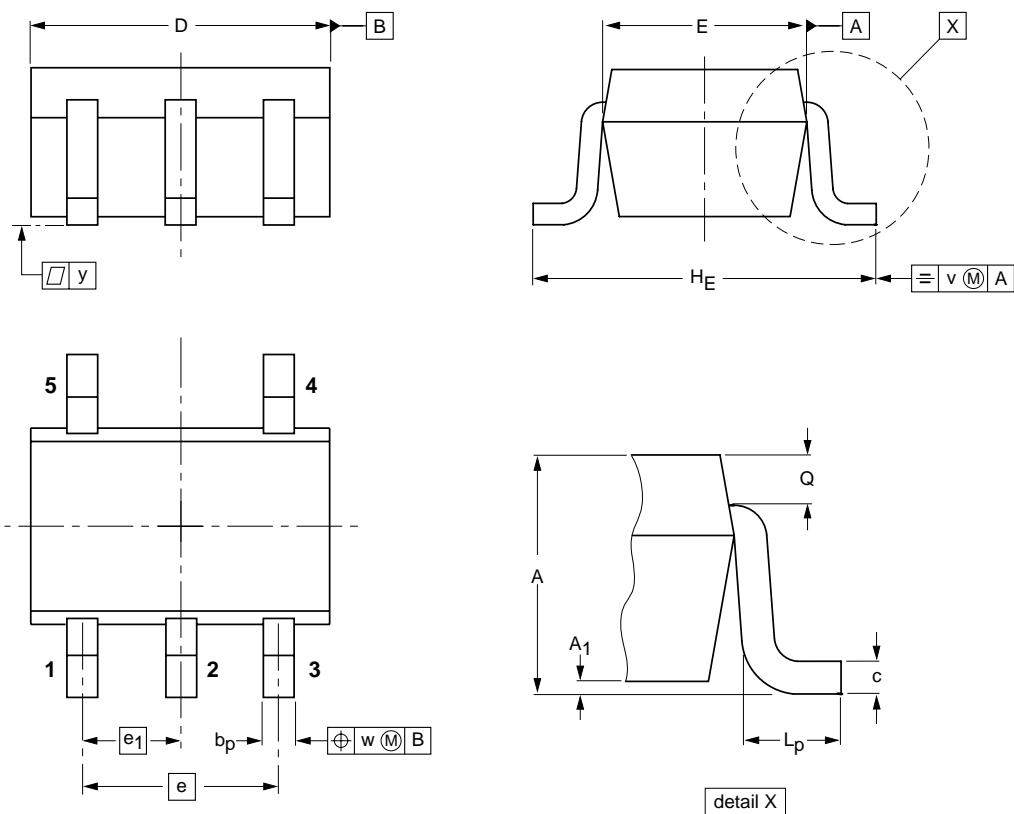
2-input NAND gate

74AHC1G00; 74AHCT1G00

PACKAGE OUTLINE

Plastic surface mounted package; 5 leads

SOT353



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E <sup>(2)</sup>	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 2-input NAND gate

## 74AHC1G00; 74AHCT1G00

## Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

## Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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