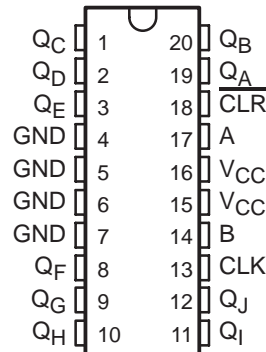


- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Fully Synchronous Data Transfers
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Pin Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR N PACKAGE  
(TOP VIEW)

## description

The 74AC11898 features AND-gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either input inhibits entry of new data and resets the first flip-flop to the low level on the rising edge of the next clock pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low provided the minimum setup and hold time requirements are met. Clocking occurs on the low-to-high transition of the clock input.

The 74AC11898 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS				OUTPUTS			
CLR	CLK	A	B	QA	QB	...	QJ
L	X	X	X	L	L		L
H	L	X	X	QA0	QB0		QJO
H	$\uparrow$	H	H	H	QAN		QIN
H	$\uparrow$	L	X	L	QAN		QIN
H	$\uparrow$	X	L	L	QAN		QIN

H = high level (steady state)

X = irrelevant (any input, including transitions)

$\uparrow$  = transition from low to high level

QA0, QB0, QJ0 = the level of QA, QB, QJ respectively, before the indicated steady-state input conditions were established.

Qn, Qin = the level of QA or QJ before the most recent  $\uparrow$  transition of the clock; indicates a one-bit shift.

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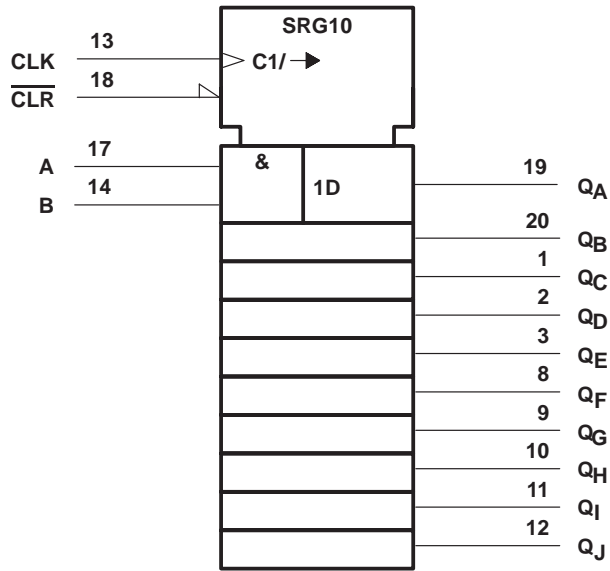
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



# 74AC11898 10-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

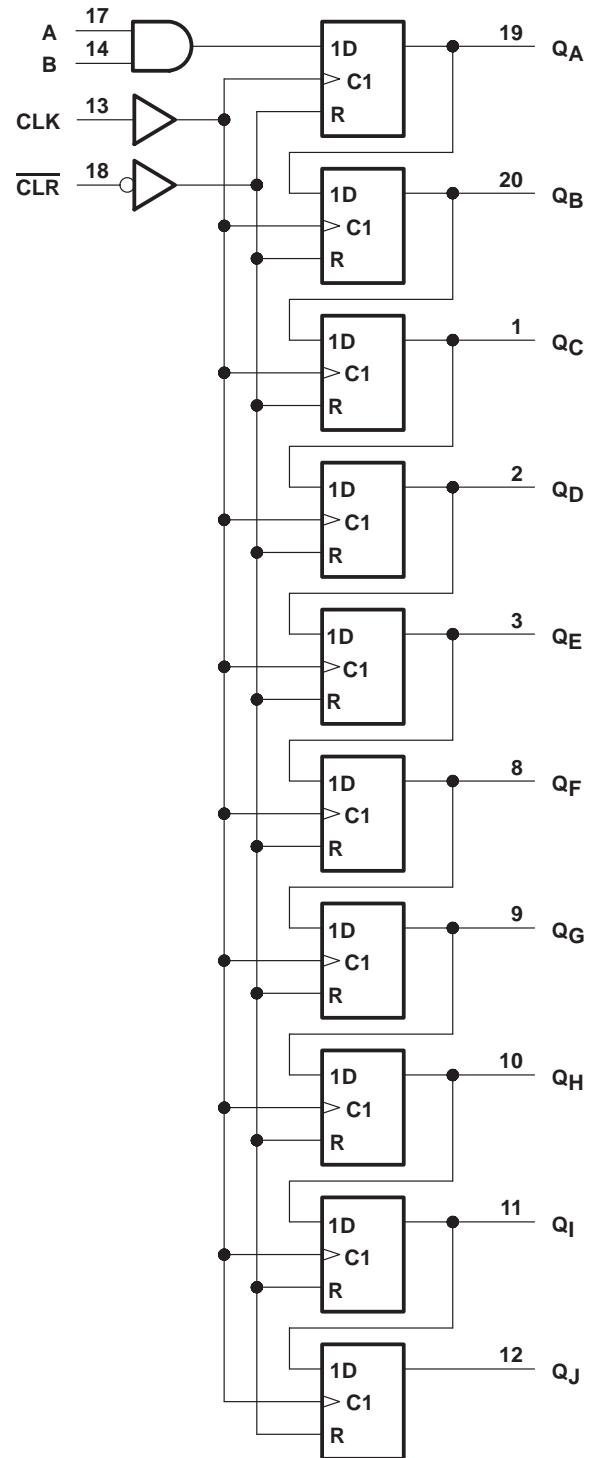
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 250$ mA
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### recommended operating conditions (see Note 2)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	3	5	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 3$ V	2.1		V
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 5.5$ V	3.85		
$V_{IL}$	Low-level input voltage	$V_{CC} = 3$ V		0.9	V
		$V_{CC} = 4.5$ V		1.35	
		$V_{CC} = 5.5$ V		1.65	
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 3$ V		-4	mA
		$V_{CC} = 4.5$ V		-24	
		$V_{CC} = 5.5$ V		-24	
$I_{OL}$	Low-level output current	$V_{CC} = 3$ V		12	mA
		$V_{CC} = 4.5$ V		24	
		$V_{CC} = 5.5$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
$T_A$	Operating free-air temperature	-40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	TA = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = - 50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I <sub>OH</sub> = - 4 mA	3 V	2.58			2.48		
		4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
I <sub>OH</sub> = - 75 mA†	5.5 V				3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	3 V				0.1		V
		4.5 V				0.1		
		5.5 V				0.1		
	I <sub>OL</sub> = 12 mA	3 V				0.36		
		4.5 V				0.36		
		5.5 V				0.36		
I <sub>OL</sub> = 75 mA†	5.5 V				1.65			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V				±0.1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V				8		μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V				4		pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER		TA = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f <sub>clock</sub>	Clock frequency	0	40	0	40	ns
t <sub>w</sub>	Pulse duration	CLR low	5	5		ns
		CLK high or low	12.5	12.5		
t <sub>su</sub>	Setup time before CLK↑	Data	14	14		ns
		CLR inactive	1.5	1.5		
t <sub>h</sub>	Hold time, data after CLK↑	0	0		ns	

timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER		TA = 25°C		MIN	MAX	UNIT
		MIN	MAX			
f <sub>clock</sub>	Clock frequency	0	60	0	60	ns
t <sub>w</sub>	Pulse duration	CLR low	4.5	4.5		ns
		CLK high or low	8.3	8.3		
t <sub>su</sub>	Setup time before CLK↑	Data	8.5	8.5		ns
		CLR inactive	1.5	1.5		
t <sub>h</sub>	Hold time, data after CLK↑	0	0		ns	

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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$f_{\text{max}}$			40	60		40		MHz
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	4.1	9.4	11.7	4.1	13	ns
$t_{\text{PLH}}$	CLK	Any Q	3.3	8.2	10.7	3.3	11.9	ns
$t_{\text{PHL}}$			3.9	8.9	10.8	3.9	12.2	

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$f_{\text{max}}$			60	90		60		MHz
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Any Q	3.8	6.7	9.1	3.8	10.3	ns
$t_{\text{PLH}}$	CLK	Any Q	2.7	5.5	7.9	2.7	8.1	ns
$t_{\text{PHL}}$			3.1	6.3	8.6	3.1	10	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

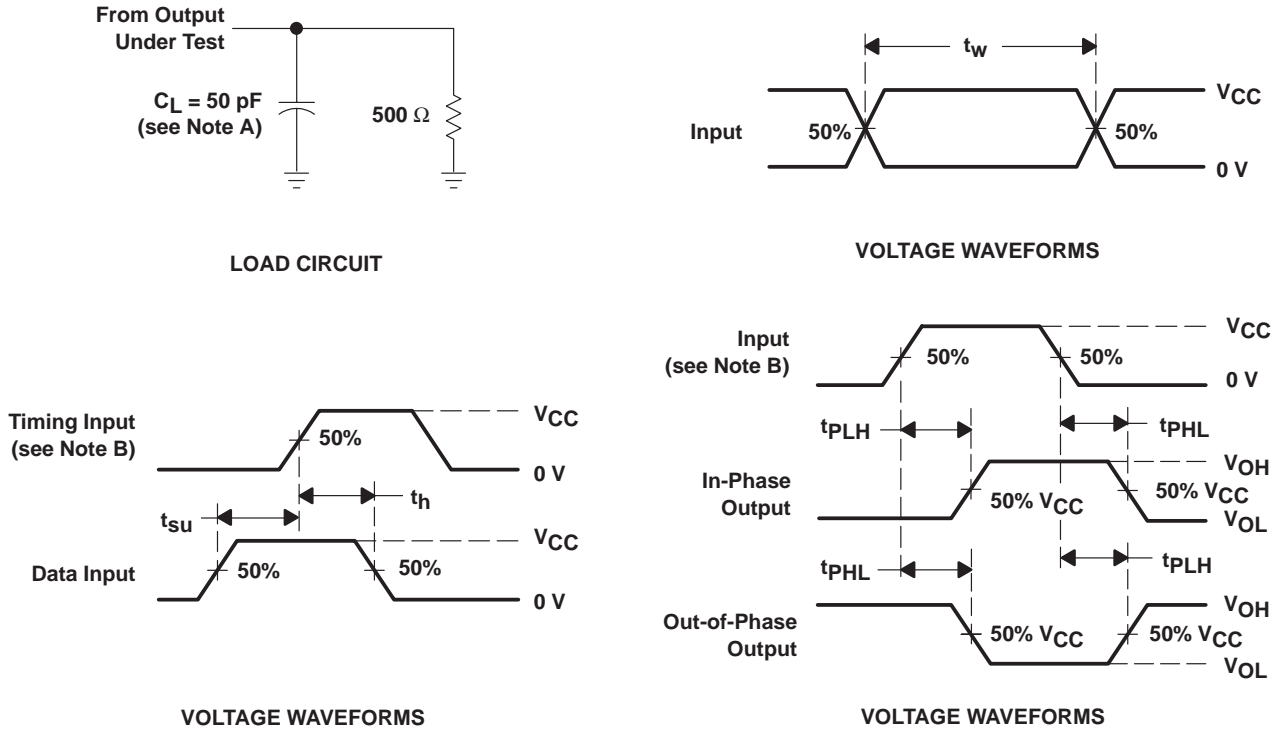
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	122	pF



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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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