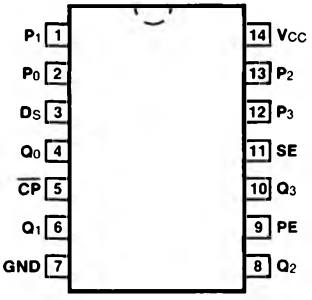
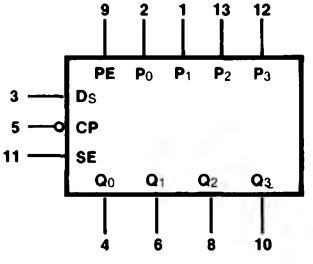
54/74178

4-BIT SHIFT REGISTER

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

DESCRIPTION — The '178 features synchronous parallel or serial entry and parallel outputs. The flip-flops are fully edge-triggered, with state changes initiated by a HIGH-to-LOW transition of the clock. Parallel Enable and Serial Enable inputs are used to select Load, Shift and Hold modes of operation. The '178 is the 14-pin version of the '179. For detail specifications, please refer to the '179 data sheet.

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74178PC		9A
Ceramic DIP (D)	A	74178DC	54178DM	6A
Flatpak (F)	A	74178FC	54178FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
PE	Parallel Enable Input	1.0/1.0
P_0 — P_3	Parallel Data Inputs	1.0/1.0
D_S	Serial Data Input	1.0/1.0
$\overline{SE}$	Shift Enable Input	1.0/1.0
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.0
Q_0 — Q_3	Flip-flop Outputs	20/10

FUNCTIONAL DESCRIPTION — The '178 contains four D-type edge-triggered flip-flops and sufficient interstage logic to perform parallel load, shift right or hold operations. All state changes are initiated by a HIGH-to-LOW transition of the clock. A HIGH signal on the Shift Enable (SE) input prevents parallel loading and permits a right shift each time the clock makes a negative transition. When the SE input is LOW, the signal applied to the Parallel Enable (PE) input determines whether the circuit is in a parallel load or a hold mode, as shown in the Mode Select Table. The SE, PE, D_S and P_n inputs can change when the clock is in either state, provided only that the recommended setup and hold times are observed.

MODE SELECT TABLE

INPUTS			RESPONSE
SE	PE	$\overline{CP}$	
H	X	⊓	Right Shift. $D_S \rightarrow Q_0$; $Q_0 \rightarrow Q_1$, etc.
L	H	⊓	Parallel load $P_n \rightarrow Q_n$.
L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM