Freescale Semiconductor
56F827 Product Brief

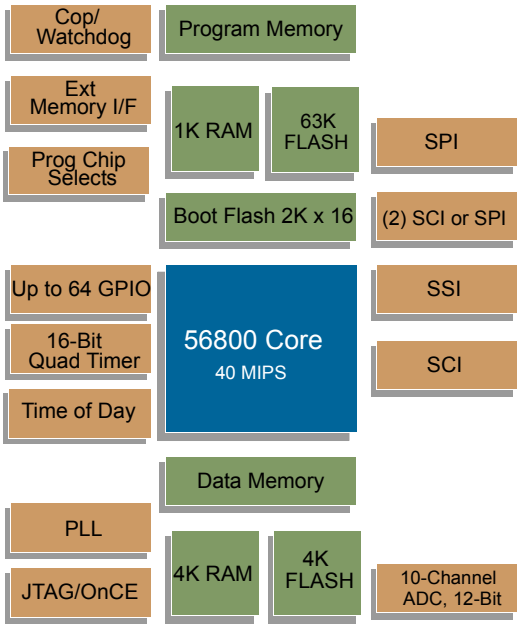
The 56F827 is a member of the 56800 core-based family of Digital Signal Controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56F827 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

BENEFITS

- Low-power applications supported by multiple operating modes
- Flash memory is engineered to provide reliable, non-volatile memory storage, eliminating the need for external storage devices
- Easy to program with flexible application development tools
- Optimized for C compiler efficiency
- Simple updating of Flash memory through SPI, SCI or OnCE™, using on-chip boot loader
- Simple interface with other asynchronous serial communication devices and off-chip EE memory
- DAC functionality available by using Quad Timer
- Sophisticated debugging using On-Chip Emulation (OnCE) to view core, peripheral, and memory contents
- ADC shutdown mode for power savings
- Program chip selects allow for enabling/disabling external memory and external peripherals

56800 CORE FEATURES

- Efficient 16-bit 56800 controller engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface



EXAMPLE APPLICATIONS

- Noise suppression
- ID tag readers
- Sonic/subsonic detectors
- Security access devices
- Remote metering
- Sonic alarms
- General purpose devices

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MEMORY FEATURES

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip Memory including a low-cost, high-volume Flash solution
  - 67K On-chip Flash
    - 63K Program Flash
    - 4K Data Flash
    - Boot via Program Flash
  - 1K Program RAM
- Off-chip memory expansion capabilities
  - As much as 64K data memory
  - As much as 64K program memory

AWARD-WINNING DEVELOPMENT ENVIRONMENT

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

56F827 PERIPHERAL CIRCUIT FEATURES

- One 10-channel, 12-bit Analog-to-Digital Converter (ADC)
- General purpose Quad Timer
- Three Serial Communication Interfaces (SCI)
- Two Serial Peripheral Interfaces (SPI)
- Synchronous Serial Interface (SSI)
- Four programmable chip selects
- 16 dedicated and 48 multiplexed GPIO pins
- Computer Operating Properly (COP)/ Watchdog timer
- Two external interrupt pins
- External reset pin for hardware reset
- JTAG/OnCE™ for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based frequency synthesizer
- One Time of Day (TOD) Timer

PRODUCT DOCUMENTATION

56800 Reference Manual	Detailed peripheral description of the 56800 architecture, 16-bit core processor and the instruction set Order Number: DSP56800FM
56F826/827 User Manual	Detailed description of memory, peripherals, and interfaces of the 56F826/827 Order Number: DSP56F826-827UM
56F827 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions Order Number: DSP56F827

ORDERING INFORMATION

PART	*DSP56F827*
PACKAGES	*128 LQFP (80 MHz)*
ORDER NUMBERS	*DSP56F827FG80*
SUPPLY VOLTAGE	*3.0V - 3.6V* *2.25V - 2.75V*

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DSP56F827PB