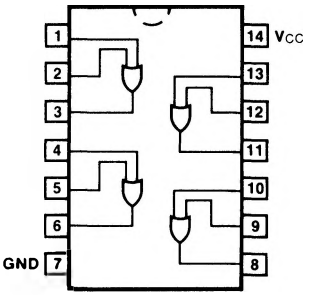
54/7432
54S/74S32
54LS/74LS32

QUAD 2-INPUT OR GATE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7432PC, 74S32PC 74LS32PC		9A
Ceramic DIP (D)	A	7432DC, 74S32DC 74LS32DC	5432DM, 54S32DM 54LS32DM	6A
Flatpak (F)	A	7432FC, 74S32FC 74LS32FC	5432FM, 54S32FM 54LS32FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	25/12.5	10/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3 for U.L. definitions

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max	Min	Max			
I_{CCH}	Power Supply Current		22		32		6.2	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			38		68		9.8		V_{IN} = Gnd	
t_{PLH}	Propagation Delay		15	2.0	7.0		15	ns	Figs. 3-1, 3-5	
t_{PHL}			22	2.0	7.0		15			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.