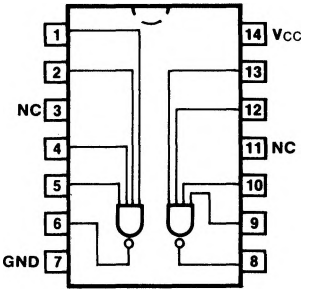
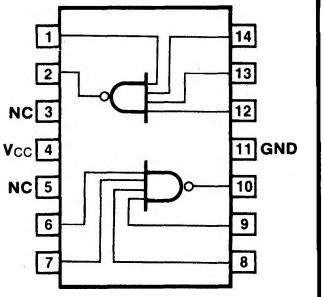
54/7422
54H/74H22
54S/74S22
54LS/74LS22

DUAL 4-INPUT NAND GATE
(With Open-Collector Output)

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7422PC, 74H22PC 74S22PC, 74LS22PC		9A
Ceramic DIP (D)	A	7422DC, 74H22DC 74S22DC, 74LS22DC	5422DM, 54H22DM 54S22DM, 54LS22DM	6A
Flatpak (F)	A	7422FC, 74S22FC 74LS22FC	5422FM, 54S22FM 54LS22FM	3I
	B	74H22FC	54H22FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	OC**/10	OC**/12.5	OC**/12.5	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74H Min	54/74H Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply		4.0		5.0		6.6		0.8	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}	Current		11		20		18		2.2		V_{IN} = Open	
t_{PLH}	Propagation Delay		45		15	2.0	7.5		22	ns	Figs. 3-2, 3-4	
t_{PHL}			15		12	2.0	7.0		18			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector