

# 54LS/74LS379

## QUAD PARALLEL REGISTER

(With Enable)

**DESCRIPTION** — The '379 is a 4-bit register with buffered common Enable. This device is similar to the '175 but features the common Enable rather than common Master Reset.

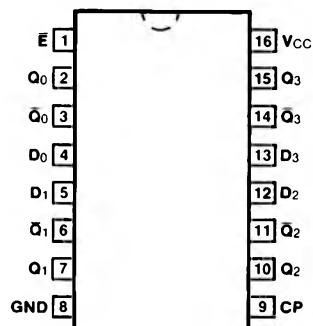
- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- BUFFERED COMMON ENABLE INPUT
- TRUE AND COMPLEMENT OUTPUTS

**ORDERING CODE:** See Section 9

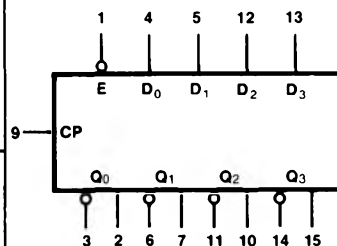
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$ , $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$ , $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74LS379PC		9B
Ceramic DIP (D)	A	74LS379DC	54LS379DM	6B
Flatpak (F)	A	74LS379FC	54LS379FM	4L

### CONNECTION DIAGRAM

#### PINOUT A



### LOGIC SYMBOL






$V_{CC} = \text{Pin } 16$   
 $GND = \text{Pin } 8$

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

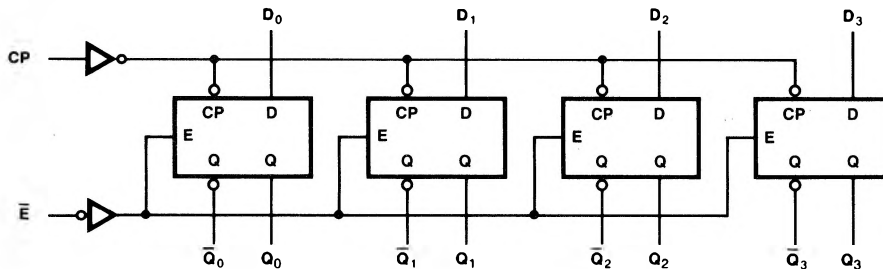
PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
$\bar{E}$	Enable Input (Active LOW)	0.5/0.25
$D_0 - D_3$	Data Inputs	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$Q_0 - Q_3$	Flip-flop Outputs	10/5.0 (2.5)
$\bar{Q}_0 - \bar{Q}_3$	Complement Outputs	10/5.0 (2.5)

**FUNCTIONAL DESCRIPTION** — The '379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock (CP) and Enable ( $\bar{E}$ ) inputs are common to all flip-flops. When the  $\bar{E}$  input is HIGH, the register will retain the present data independent of the CP input. The  $D_n$  and  $\bar{E}$  inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

**TRUTH TABLE**

INPUTS			OUTPUTS	
$\bar{E}$	CP	$D_n$	$Q_n$	$\bar{Q}_n$
H		X	No Change	No Change
L		H	H	L
L		L	L	H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

**LOGIC DIAGRAM**

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I <sub>CC</sub>	Power Supply Current	18		mA	V <sub>CC</sub> = Max

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF			
		Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	30		MHz	Figs. 3-1, 3-8
t <sub>PLH</sub>	Propagation Delay	27		ns	
t <sub>PHL</sub>	CP to Q <sub>n</sub>	27			

**AC OPERATING REQUIREMENTS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t <sub>s</sub> (H)	Setup Time HIGH or LOW	20		ns	Fig. 3-6
t <sub>s</sub> (L)	D <sub>n</sub> to CP	20			
t <sub>h</sub> (H)	Hold Time HIGH or LOW	5.0		ns	
t <sub>h</sub> (L)	D <sub>n</sub> to CP	5.0			
t <sub>s</sub> (H)	Setup Time HIGH or LOW	25		ns	
t <sub>s</sub> (L)	$\bar{E}$ to CP	25			
t <sub>h</sub> (H)	Hold Time HIGH or LOW	5.0		ns	
t <sub>h</sub> (L)	$\bar{E}$ to CP	5.0			
t <sub>w</sub> (L)	CP Pulse Width LOW	17		ns	Fig. 3-8