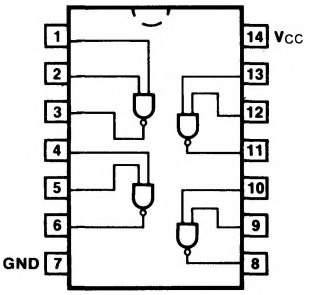
54/7437
54LS/74LS37
QUAD 2-INPUT NAND BUFFER

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°c to +125°C	PKG TYPE
Plastic DIP (P)	A	7437PC, 74LS37PC		9A
Ceramic DIP (D)	A	7437DC, 74LS37DC	5437DM, 54LS37DM	6A
Flatpak (F)	A	7437FC, 74LS37FC	5437FM, 54LS37FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	30/30	30/15 (7.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER		54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.4		2.5		V	V_{CC} = Max, I_{OH} = -1.2 mA V_{IN} = V_{IL}	
		XC	2.4		2.7				
V_{OL}	Output LOW Voltage	XM, XC		0.4			V	I_{OL} = 48 mA	V_{CC} = Min V_{IN} = 2.0 V
		XM				0.4		I_{OL} = 12 mA	
		XC				0.5		I_{OL} = 24 mA	
I_{OS}	Output Short Circuit Current	XM	-20	-70	-30	-130	mA	V_{CC} = Min, V_{OUT} = 0 V	
		XC	-18	-70	-30	-130			
I_{CCH} I_{CCL}	Power Supply Current			15.5 54		2.0 12	mA	V_{IN} = Gnd V_{IN} = Open	V_{CC} = Max
t_{PLH} t_{PHL}	Propagation Delay			22 15		20 20	ns	Figs. 3-1, 3-4	

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.