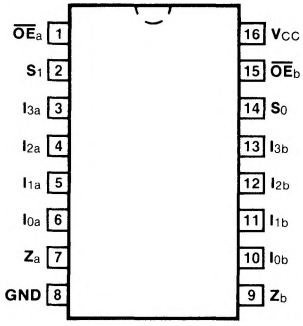
54S/74S253
54LS/74LS253

DUAL 4-INPUT MULTIPLEXER
(With 3-State Outputs)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Fairchild TTL families.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING 3-STATE OUTPUTS**

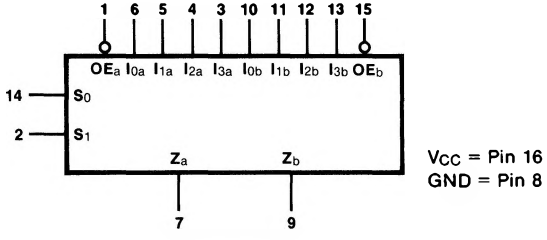
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S253PC, 74LS253PC		9B
Ceramic DIP (D)	A	74S253DC, 74LS253DC	54S253DM, 54LS253DM	6B
Flatpak (F)	A	74S253FC, 74LS253FC	54S253FM, 54LS253FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	1.25/1.25	0.5/0.25
I_{0b} — I_{3b}	Side B Data Inputs	1.25/1.25	0.5/0.25
S_0, S_1	Common Select Inputs	1.25/1.25	0.5/0.25
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	1.25/1.25	0.5/0.25
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	1.25/1.25	0.5/0.25
Z_a, Z_b	3-State Outputs	162/12.5 (50)	65/5.0 (25)/(2.5)

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — This device contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which when HIGH, force the outputs to a high impedance (high Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

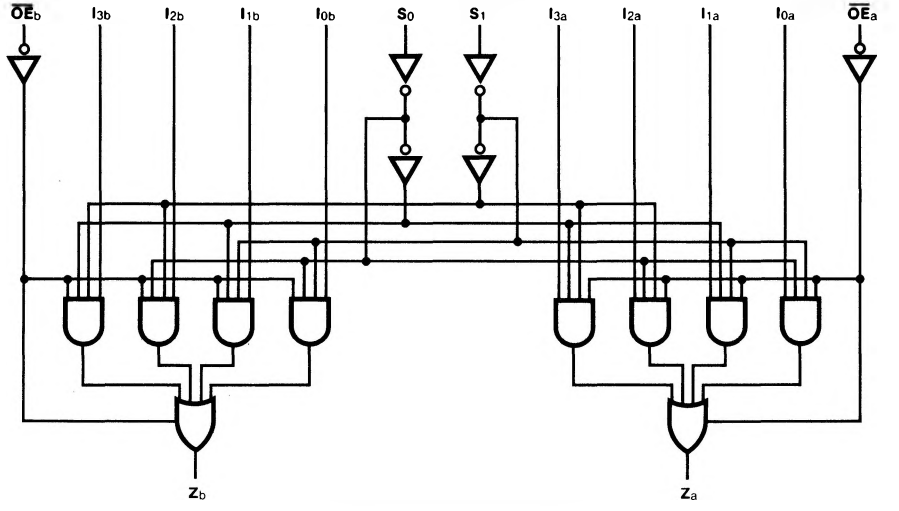
If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{OS}	Output Short Circuit Current		-40	-100	-20	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current	Outputs HIGH		70			mA	V_{CC} = Max, $\overline{OE}_n$ = Gnd I_n, S_n = 4.5 V
		Outputs LOW		80		12		V_{CC} = Max I_n, S_n, $\overline{OE}_n$ = Gnd
		Outputs OFF		100		14		V_{CC} = Max, $\overline{OE}_n$ = 4.5 V I_n, S_n = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74S C_L = 15 pF, R_L = 280 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n		18 18		29 24	ns	Figs. 3-1, 3-20
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n		9.0 9.0		20 15	ns	Figs. 3-1, 3-5
t_{PZH} t_{PZL}	Output Enable Time		19.5 21		22 22	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, C_L = 15 pF ('LS253); C_L = 50 pF ('S253)
t_{PHZ} t_{PLZ}	Output Disable Time		8.5 14		32 22	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ, ('LS253) C_L = 5 pF