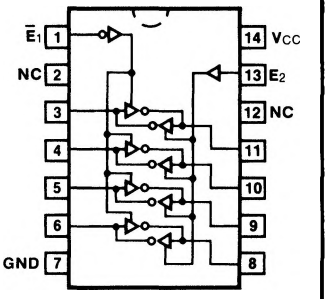
54LS/74LS242
54LS/74LS243

QUAD BUS TRANSCEIVER

(With 3-State Outputs)

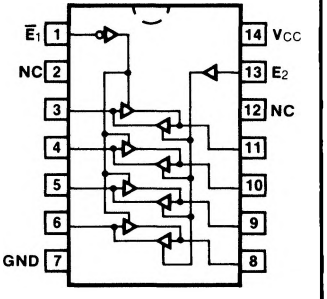
CONNECTION DIAGRAMS
PINOUT A



DESCRIPTION — The 'LS242 and '243 are quad bus transmitters/receivers designed for 4-line asynchronous 2-way data communications between data buses.

- **HYSTERESIS AT INPUTS TO IMPROVE NOISE IMMUNITY**
- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **FULLY TTL AND CMOS COMPATIBLE**

PINOUT B



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS242PC		9A
	B	74LS243PC		
Ceramic DIP (D)	A	74LS242DC	54LS242DM	6A
	B	74LS243DC	54LS243DM	
Flatpak (F)	A	74LS242FC	54LS242FM	3I
	B	74LS243FC	54LS243FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.125
Outputs	75/15 (7.5)

TRUTH TABLES

'LS242

INPUTS		OUTPUT
$\overline{E}_1$	D	
L	L	H
L	H	L
H	X	Z
H	X	Z

INPUTS		OUTPUT
E_2	D	
L	X	Z
L	X	Z
H	L	H
H	H	L

'LS243

INPUTS		OUTPUT
$\overline{E}_1$	D	
L	L	L
L	H	H
H	X	Z
H	X	Z

INPUTS		OUTPUT
E_2	D	
L	X	Z
L	X	Z
H	L	L
H	H	H

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage	XM	2.0		V	I_{OH} = -12 mA	V_{CC} = Min, V_{IH} = 2.0 V, V_{IL} = 0.5 V
		XC	2.0			I_{OH} = -15 mA	
V_{OH}	Output HIGH Voltage		2.4		V	I_{OH} = -3.0 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} per Truth Table	
I_{OS}	Output Short Circuit Current		-40	-225	mA	V_{CC} = Max, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	HIGH		38	mA	V_{CC} = Max	
		LOW		50			
		OFF ('242)		50			
		OFF ('243)		54			

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 45 pF Min	54/74LS C_L = 45 pF Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('242)		14 18	ns	Figs. 3-1, 3-4
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('243)		18 18	ns	Figs. 3-1, 3-5
t_{PZH} t_{PZL}	Output Enable Time		23 30	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω
t_{PLZ} t_{PHZ}	Output Disable Time		25 18	ns	Figs. 3-3, 3-11, 3-12 R_L = 667 Ω, C_L = 5 pF