

54FCT/74FCT825A • 54FCT/74FCT825B

8-Bit D Flip-Flop

General Description

The FCT825A/B is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

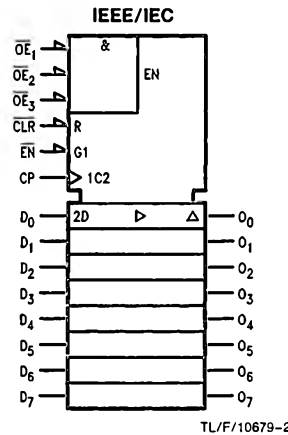
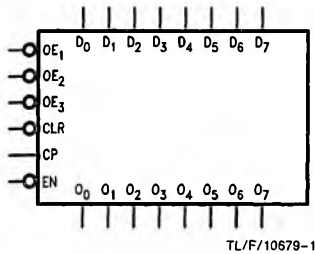
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

- ▣ NSC 54FCT/74FCT825A/B is pin and functionally equivalent to IDT 54FCT/74FCT825A/B
- ▣ High-speed parallel registers with positive edge-triggered D-type flip flops
- ▣ Buffered common clock enable (\overline{EN}) and asynchronous Clear input (CLR)
- ▣ Input clamp diodes to limit bus reflections
- ▣ TTL/CMOS input and output level compatible
- ▣ $I_{OL} = 48 \text{ mA (Com)}, 32 \text{ mA (Mil)}$
- ▣ CMOS power levels
- ▣ 4 kV minimum ESD immunity
- ▣ Military Product compliant to MIL-STD 883

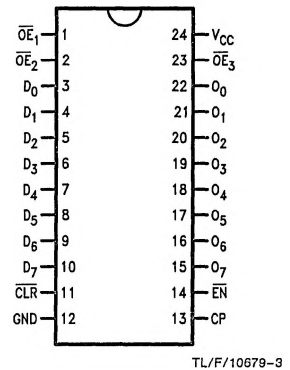
Logic Symbols



Pin Names	Description
D ₀ -D ₇	Data Inputs
O ₀ -O ₇	Data Outputs
$\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$	Output Enables
EN	Clock Enable
CLR	Clear
CP	Clock Input

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

