National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT823A • 54FCT/74FCT823B
9-Bit D Flip-Flop

General Description

The 'FCT823A/B is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

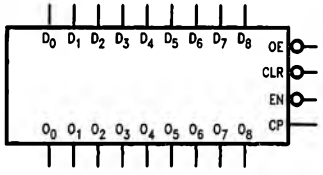
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT823A/B is pin and functionally equivalent to IDT 54FCT/74ACT823A/B
- High speed parallel registers with positive edge-triggered D-type flip-flop
- Buffered common clock enable ($\overline{EN}$) and asynchronous clear input (CLR)
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD 883

Logic Symbols



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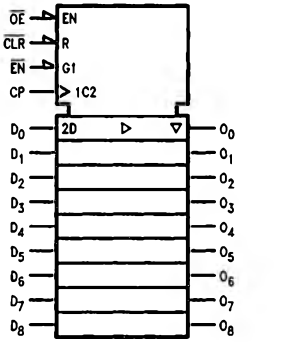
Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
CP	Clock Input
$\overline{EN}$	Clock Enable

IEEE/IEC



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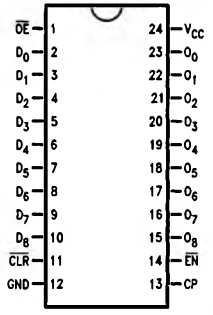
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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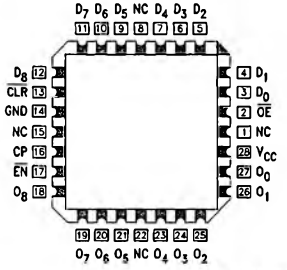
Pin Assignment for LCC



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