

# 54FCT574

*54FCT574 Octal D-Type Flip-Flop with -TRISTATE Outputs*



Literature Number: SNOS429

## 54FCT574

### Octal D-Type Flip-Flop with TRI-STATE® Outputs

#### General Description

The 'FCT574 is an octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ( $\overline{OE}$ ). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The device is functionally identical to the 'FCT374 except for the pinouts.

#### Features

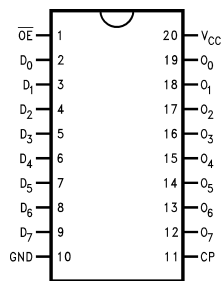
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'FCT374
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 32 mA, source capability of 12 mA
- TTL input and output level compatible
- CMOS power consumption
- Standard Microcircuit Drawing (SMD) 5962-8951301

#### Ordering Code

Military	Package Number	Package Description
54FCT574DMQB	J20A	20-Lead Ceramic Dual-In-Line
54FCT574FMQB	W20A	20-Lead Cerpack
54FCT574LMQB	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

#### Connection Diagrams

Pin Assignment for DIP and Flatpak

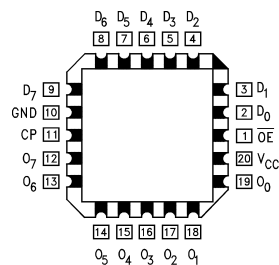


DS100966-1

#### Pin Descriptions

Pin Names	Description
$D_0-D_7$	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
$O_0-O_7$	TRI-STATE Outputs

Pin Assignment for LCC



DS100966-2

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## Functional Description

The 'FCT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs are in a high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

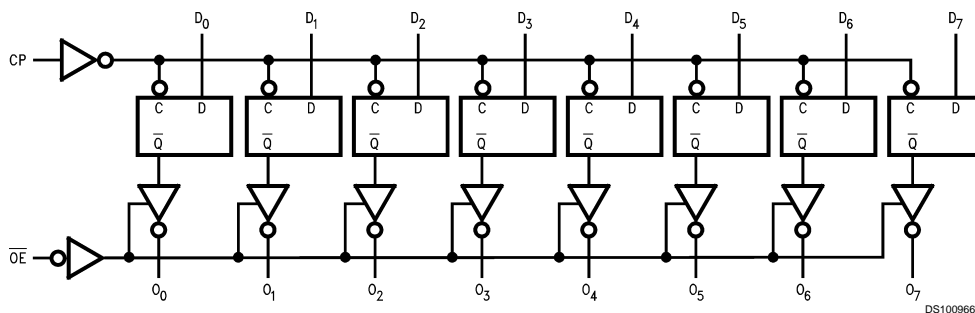
Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H or L	H	NC	Z	Hold
H	N	L	L	Z	Load
H	N	H	H	Z	Load
L	N	L	L	L	Data Available
L	N	H	H	H	Data Available
L	H or L	L	NC	NC	No Change in Data
L	H or L	H	NC	NC	No Change in Data

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 N = LOW-to-HIGH Transition  
 NC = No Change

## Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H or L	L	NC	Z	Hold

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State in the HIGH State	-0.5V to 5.5V -0.5V to V <sub>CC</sub>

Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current	-500 mA

**Recommended Operating Conditions**

Free Air Ambient Temperature	
Military	-55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	FCT574		Units	V <sub>CC</sub>	Conditions
		Min	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0		V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage		0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage		-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54FCT	4.3	V	Min	I <sub>OH</sub> = -300 μA
		54FCT	2.4	V	Min	I <sub>OH</sub> = -12 mA
V <sub>OL</sub>	Output LOW Voltage	54FCT	0.2	V	Min	I <sub>OL</sub> = 300 μA
		54FCT	0.5	V	Min	I <sub>OL</sub> = 32mA
I <sub>IH</sub>	Input HIGH Current		5	μA	Max	V <sub>IN</sub> = 2.7V (Note 3)
			5	μA	Max	V <sub>IN</sub> = V <sub>CC</sub>
I <sub>IL</sub>	Input LOW Current		-5	μA	Max	V <sub>IN</sub> = 0.5V (Note 3)
			-5	μA	Max	V <sub>IN</sub> = 0.0V
I <sub>OZH</sub>	Output Leakage Current		10	μA	0 – 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}$ = 2.0V
I <sub>OZL</sub>	Output Leakage Current		-10	μA	0 – 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}$ = 2.0V
I <sub>OS</sub>	Output Short-Circuit Current		-60	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CCQ</sub>	Power Supply Current		1.5	mA	Max	V <sub>IN</sub> = 0.2V or V <sub>IN</sub> = 5.3V, f <sub>I</sub> = 0MHz
ΔI <sub>CC</sub>	Power Supply Current		2.0	mA	Max	V <sub>IN</sub> = 3.4V
I <sub>CCT</sub>	Additional I <sub>CC</sub> /Input		6.0	mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V or V <sub>IN</sub> = GND, f <sub>CP</sub> = 10MHz, Outputs open, $\overline{OE}$ = GND, one bit toggling at f <sub>I</sub> = 5MHz, 50% duty cycle
			5.5	mA	Max	V <sub>I</sub> = 5.3V or V <sub>CC</sub> = 0.2V, f <sub>CP</sub> = 10MHz, Outputs open, $\overline{OE}$ = GND, one bit toggling at f <sub>I</sub> = 5MHz, 50% duty cycle
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> No Load		0.40	mA/MHz	Max	Outputs Open, $\overline{OE}$ = GND, One bit toggling, 50% duty cycle, V <sub>IN</sub> = 5.3V or V <sub>IN</sub> = 0.2V

**Note 3:** Guaranteed, but not tested.

AC Electrical Characteristics					
Symbol	Parameter	54FCT		Units	Fig. No.
		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF			
		Min	Max		
t <sub>PLH</sub>	Propagation Delay	2.0	11.0	ns	Figure 4
t <sub>PHL</sub>	CP to O <sub>n</sub>	2.0	11.0		
t <sub>PZH</sub>	Output Enable Time	1.5	14.0	ns	Figure 6
t <sub>PZL</sub>		1.5	14.0		
t <sub>PHZ</sub>	Output Disable Time	1.5	8.0	ns	Figure 6
t <sub>PLZ</sub>		1.5	8.0		

AC Operating Requirements					
Symbol	Parameter	54FCT		Units	Fig. No.
		T <sub>A</sub> = -55°C to +125°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF			
		Min	Max		
t <sub>s</sub> (H)	Setup Time, HIGH	3.5		ns	Figure 7
t <sub>s</sub> (L)	or LOW D <sub>n</sub> to CP	3.5			
t <sub>h</sub> (H)	Hold Time, HIGH	2.0		ns	Figure 7
t <sub>h</sub> (L)	or LOW D <sub>n</sub> to CP	2.0			
t <sub>w</sub> (H)	Pulse Width, CP,	7.0		ns	Figure 5
t <sub>w</sub> (L)	HIGH or LOW	7.0			

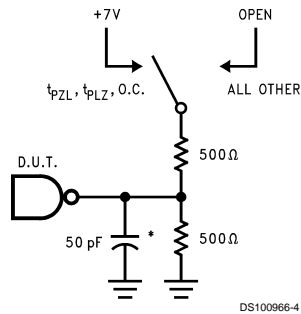
  

### Capacitance

Symbol	Parameter	Typ	Units	Conditions T <sub>A</sub> = 25°C
C <sub>IN</sub>	Input Capacitance	5.0	pF	V <sub>CC</sub> = 0V
C <sub>OUT</sub> (Note 4)	Output Capacitance	9.0	pF	V <sub>CC</sub> = 5.0V

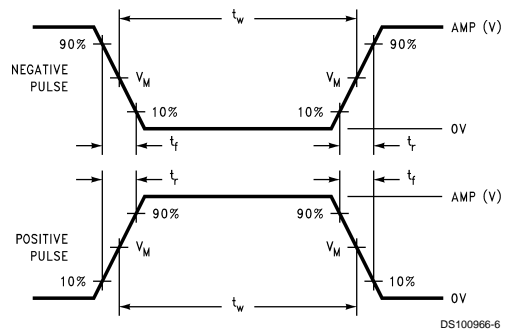
**Note 4:** C<sub>OUT</sub> is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

### AC Loading



\*Includes jig and probe capacitance

**FIGURE 1. Standard AC Test Load**

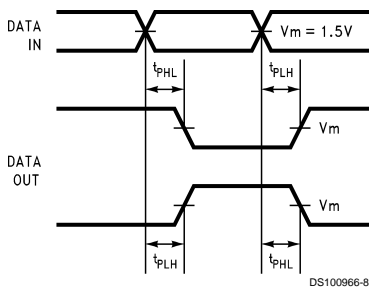


**FIGURE 2.  $V_M = 1.5V$**

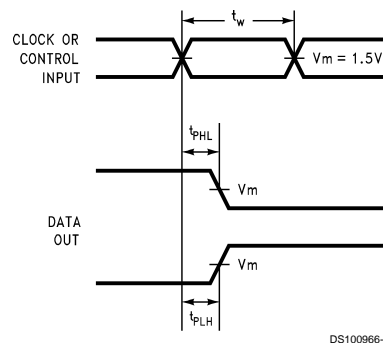
### Input Pulse Requirements

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

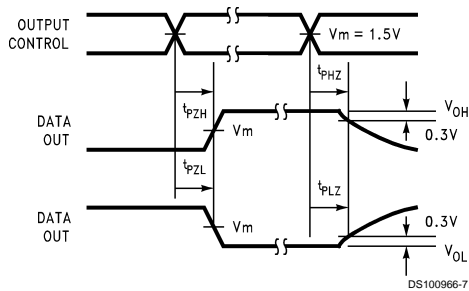
**FIGURE 3. Test Input Signal Requirements**



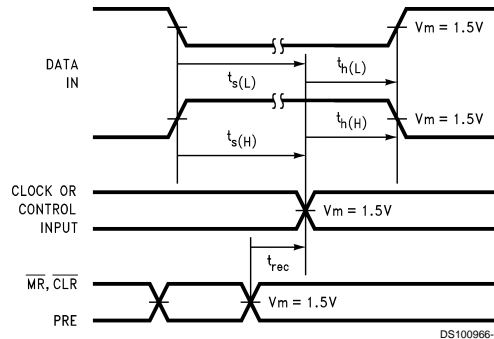
**FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



**FIGURE 5. Propagation Delay, Pulse Width Waveforms**

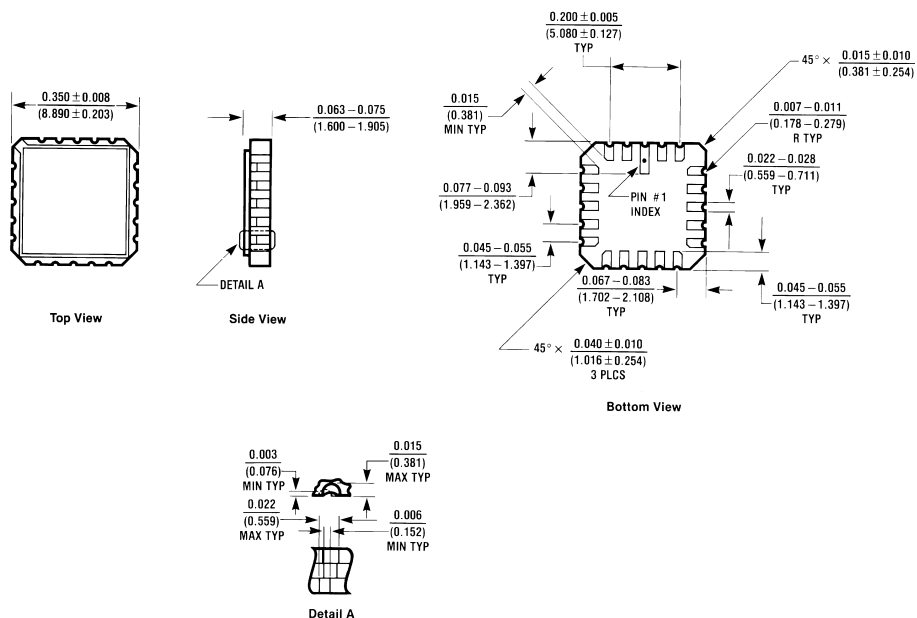


**FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times**



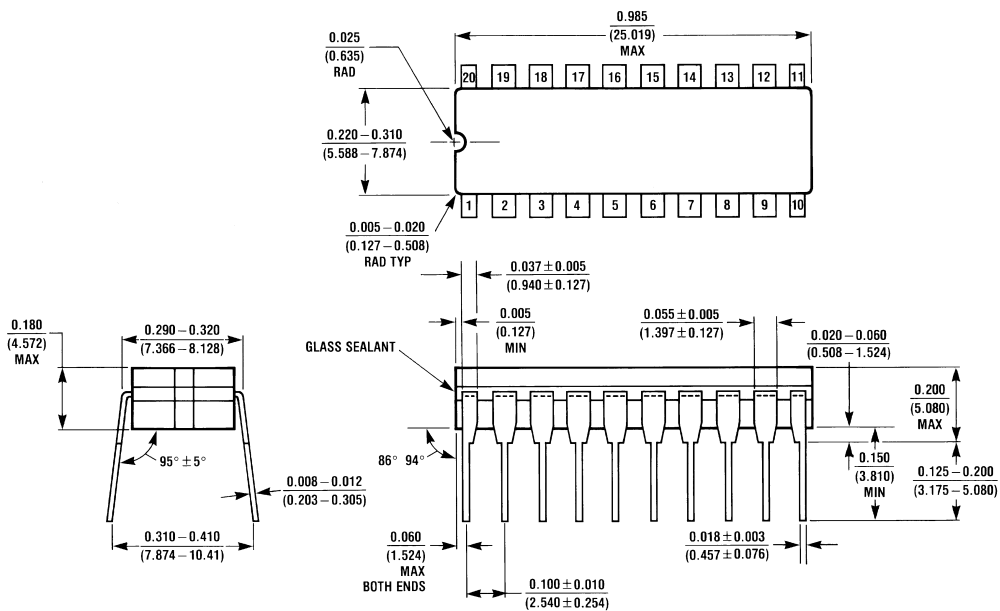
**FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms**

**Physical Dimensions** inches (millimeters) unless otherwise noted



E20A (REV D)

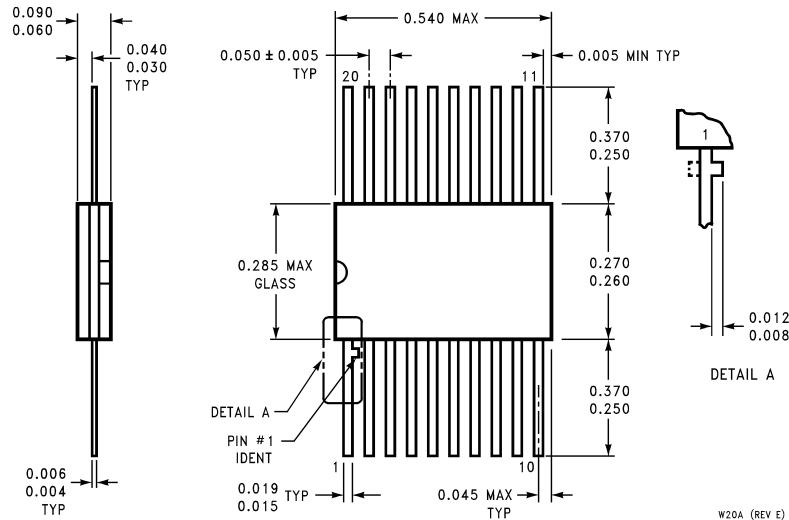
**20-Terminal Ceramic Chip Carrier (L)**  
NS Package Number E20A



J20A (REV M)

**20-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J20A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Ceramic Flatpak (F)  
NS Package Number W20A**

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