National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT273A
Octal D Flip-Flop

General Description

The 'FCT273A has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

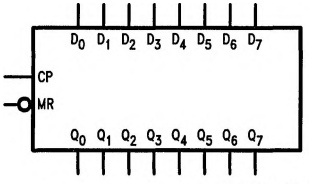
FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features NSC correction and split ground bus for superior performance.

Features

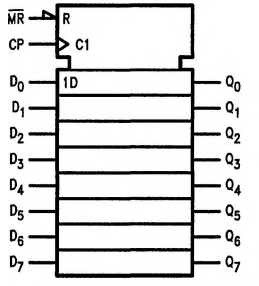
- NSC 54FCT/74FCT273A is pin and functionally equivalent to IDT 54FCT/74FCT273A
- Ideal buffer for MOS microprocessor or memory
- Buffered common clock
- Buffered, asynchronous master reset
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



TL/F/10660–1

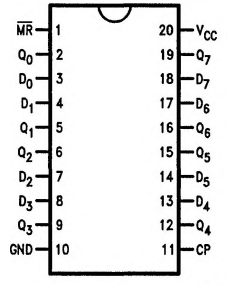
IEEE/IEC



TL/F/10660–2

Connection Diagrams

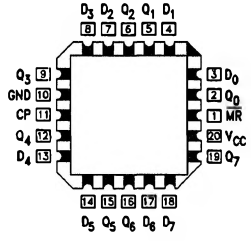
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10660–3

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

Pin Assignment for LCC



TL/F/10660–4