National Semiconductor

54F/74F632
32-Bit Parallel Error Detection and Correction Circuit

General Description

The 'F632 device is a 32-bit parallel error detection and correction circuit (EDAC) in a 52-pin or 68-pin package. The EDAC uses a modified Hamming code to generate a 7-bit check word from a 32-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 39-bit words from memory are processed by the EDAC to determine if errors have occurred in memory.

Single-bit errors in the 32-bit data word are flagged and corrected.

Single-bit errors in the 7-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 32-bit data word is not in error. The correction cycle will simply pass along the original 32-bit data word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These errors may occur in any two bits of the 39-bit word from memory (two errors in the 32-bit data word, two errors in the 7-bit check word, or one error in each word). The gross-error condition of all LOWs or all HIGHs from memory will be detected. Otherwise, errors in three or more bits of the 39-bit word are beyond the capabilities of these devices to detect.

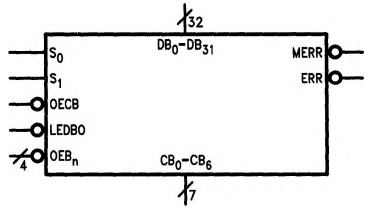
Read-modify-write (byte-control) operations can be performed by using output latch enable, $\overline{LEDBO}$, and the individual $\overline{OEB}_0$ through $\overline{OEB}_3$ byte control pins.

Diagnostics are performed on the EDACs by controls and internal paths that allow the user to read the contents of the Data Bit and Check Bit input latches. These will determine if the failure occurred in memory or in the EDAC.

Features

- Detects and corrects single-bit errors
- Detects and flags dual-bit errors
- Built-in diagnostic capability
- Fast write and read cycle processing times
- Byte-write capability

Logic Symbol



TL/F/9579–1

Unit Loading/Fan Out: See Section 1 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CB_0–CB_6	Check Word Bit, Input	3.5/1.083	70 μA/−650 μA
	or TRI-STATE® Output	150/40 (33.3)	−3 mA/24 mA (20 mA)
DB_0–DB_{31}	Data Word Bit, Input	3.5/1.083	70 μA/−650 μA
	or TRI-STATE Output	150/40 (33.3)	−3 mA/24 mA (20 mA)
$\overline{OEB}_0$–$\overline{OEB}_3$	Output Enable Data Bits	1.0/1.0	20 μA/−0.6 mA
$\overline{LEDBO}$	Output Latch Enable Data Bit	1.0/1.0	20 μA/−0.6 mA
$\overline{OECB}$	Output Enable Check Bit	1.0/1.0	20 μA/−0.6 mA
S_0, S_1	Select Pins	1.0/1.0	20 μA/−0.6 mA
$\overline{ERR}$	Single Error Flag	50/33.3	−1 mA/20 mA
$\overline{MERR}$	Multiple Error Flag	50/33.3	−1 mA/20 mA