54AC374,54ACT374

54AC374 54ACT374 Octal D Flip-Flop with TRI-STATE Outputs

TEXAS INSTRUMENTS

Literature Number: SNOS105

National Semiconductor

August 1998

54AC374 • 54ACT374
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'AC/'ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- See '273 for reset version
- See '377 for clock enable version
- See '373 for transparent latch version
- See '574 for broadside pinout version
- See '564 for broadside pinout version with inverted outputs
- 'ACT374 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'AC374: 5962-87694
  — 'ACT374: 5962-87631

Logic Symbols

DS100289-1

IEEE/IEC

DS100289-2
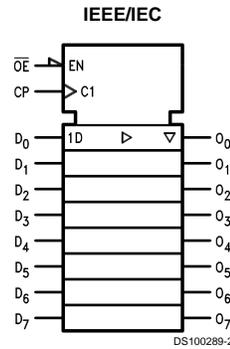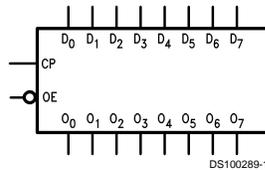
Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Connection Diagrams

Pin Assignment for DIP and Flatpak

```
         ┌──────⌣──────┐
   OE ─┤ 1         20 ├─ V_CC
   O_0 ─┤ 2         19 ├─ O_7
   D_0 ─┤ 3         18 ├─ D_7
   D_1 ─┤ 4         17 ├─ D_6
   O_1 ─┤ 5         16 ├─ O_6
   O_2 ─┤ 6         15 ├─ O_5
   D_2 ─┤ 7         14 ├─ D_5
   D_3 ─┤ 8         13 ├─ D_4
   O_3 ─┤ 9         12 ├─ O_4
  GND ─┤ 10        11 ├─ CP
         └─────────────┘
            DS100289-3
```

Pin Assignment for LCC

```
        D_3  D_2  O_2  O_1  D_1
        [8]  [7]  [6]  [5]  [4]

  O_3 [9]                    [3] D_0
 GND [10]                    [2] O_0
  CP [11]                    [1] OE
  O_4 [12]                   [20] V_CC
  D_4 [13]                   [19] O_7

       [14] [15] [16] [17] [18]
        D_5  O_5  O_6  D_6  D_7
```

DS100289-4
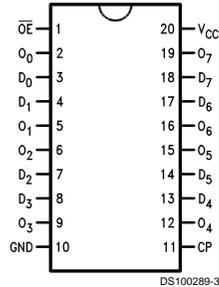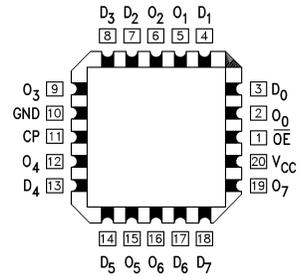
Functional Description

The 'AC/'ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition

Logic Diagram

DS100289-5
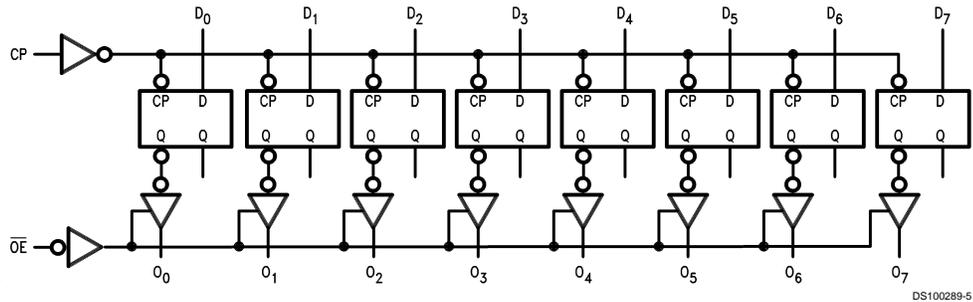
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions	
V_{IH}	Minimum High	3.0	2.1		V_{OUT} = 0.1V	
	Level Input	4.5	3.15	V	or V_{CC} − 0.1V	
	Voltage	5.5	3.85			
V_{IL}	Maximum Low	3.0	0.9		V_{OUT} = 0.1V	
	Level Input	4.5	1.35	V	or V_{CC} − 0.1V	
	Voltage	5.5	1.65			
V_{OH}	Minimum High	3.0	2.9		I_{OUT} = −50 µA	
	Level Output	4.5	4.4	V		
	Voltage	5.5	5.4			
					(Note 2) V_{IN} = V_{IL} or V_{IH}	
		3.0	2.4			−12 mA
		4.5	3.7	V	I_{OH}	−24 mA
		5.5	4.7			−24 mA
V_{OL}	Maximum Low	3.0	0.1		I_{OUT} = 50 µA	
	Level Output	4.5	0.1	V		
	Voltage	5.5	0.1			
					(Note 2) V_{IN} = V_{IL} or V_{IH}	
		3.0	0.50			12 mA
		4.5	0.50	V	I_{OL}	24 mA
		5.5	0.50			24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND	
I_{OZ}	Maximum TRI-STATE Current	5.5	±5.0	µA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND	

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V$_{CC}$ (V)	54AC T$_A$ = −55°C to +125°C Guaranteed Limits	Units	Conditions
I$_{OLD}$	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V$_{OLD}$ = 1.65V Max
I$_{OHD}$		5.5	−50	mA	V$_{OHD}$ = 3.85V Min
I$_{CC}$	Maximum Quiescent Supply Current	5.5	80.0	µA	V$_{IN}$ = V$_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I$_{IN}$ and I$_{CC}$ @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V$_{CC}$.
I$_{CC}$ for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V$_{CC}$ (V)	54ACT T$_A$ = −55°C to +125°C Guaranteed Limits	Units	Conditions
V$_{IH}$	Minimum High Level Input Voltage	4.5	2.0	V	V$_{OUT}$ = 0.1V
		5.5	2.0		or V$_{CC}$ − 0.1V
V$_{IL}$	Maximum Low Level Input Voltage	4.5	0.8	V	V$_{OUT}$ = 0.1V
		5.5	0.8		or V$_{CC}$ − 0.1V
V$_{OH}$	Minimum High Level Output Voltage	4.5	4.4	V	I$_{OUT}$ = −50 µA
		5.5	5.4		
		4.5	3.70	V	(Note 5) V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OH}$ −24 mA
		5.5	4.70		−24 mA
V$_{OL}$	Maximum Low Level Output Voltage	4.5	0.1	V	I$_{OUT}$ = 50 µA
		5.5	0.1		
		4.5	0.50	V	(Note 5) V$_{IN}$ = V$_{IL}$ or V$_{IH}$ I$_{OL}$ 24 mA
		5.5	0.50		24 mA
I$_{IN}$	Maximum Input Leakage Current	5.5	±1.0	µA	V$_I$ = V$_{CC}$, GND
I$_{OZ}$	Maximum TRI-STATE Current	5.5	±5.0	µA	V$_I$ = V$_{IL}$, V$_{IH}$ V$_O$ = V$_{CC}$, GND
I$_{CCT}$	Maximum I$_{CC}$/Input	5.5	1.6	mA	V$_I$ = V$_{CC}$ − 2.1V
I$_{OLD}$	(Note 6) Minimum Dynamic Output Current	5.5	50	mA	V$_{OLD}$ = 1.65V Max
I$_{OHD}$		5.5	−50	mA	V$_{OHD}$ = 3.85V Min
I$_{CC}$	Maximum Quiescent Supply Current	5.5	80.0	µA	V$_{IN}$ = V$_{CC}$ or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Note 7: I$_{CC}$ for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 8)	54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock Frequency	3.3	60		MHz	
		5.0	95			
t_{PLH}	Propagation Delay CP to O_n	3.3	3.0	16.5	ns	
		5.0	3.0	12.0		
t_{PHL}	Propagation Delay CP to O_n	3.3	3.0	15.0	ns	
		5.0	3.0	11.0		
t_{PZH}	Output Enable Time	3.3	1.0	14.0	ns	
		5.0	1.5	10.5		
t_{PZL}	Output Enable Time	3.3	1.0	14.0	ns	
		5.0	1.5	10.5		
t_{PHZ}	Output Disable Time	3.3	1.0	16.0	ns	
		5.0	1.5	12.5		
t_{PLZ}	Output Disable Time	3.3	1.0	13.0	ns	
		5.0	1.5	10.5		

Note 8: Voltage Range 3.3 is 3.3V ±0.3V

Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 9)	54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW D_n to CP	3.3	6.5	ns	
		5.0	5.0		
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	1.0	ns	
		5.0	1.5		
t_w	CP Pulse Width, HIGH or LOW	3.3	6.5	ns	
		5.0	5.0		

Note 9: Voltage Range 3.3 is 3.3V ±0.3V

Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 10)	54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		Units
			Min	Max	
f_{max}	Maximum Clock Frequency	5.0	70		MHz
t_{PLH}	Propagation Delay CP to O_n	5.0	1.5	12.0	ns
t_{PHL}	Propagation Delay CP to O_n	5.0	1.5	11.5	ns
t_{PZH}	Output Enable Time	5.0	1.5	11.5	ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	V$_{CC}$ (V) (Note 10)	54ACT T$_A$ = −55°C to +125°C C$_L$ = 50 pF		Units
			Min	Max	
t$_{PZL}$	Output Enable Time	5.0	1.5	11.5	ns
t$_{PHZ}$	Output Disable Time	5.0	1.5	13.0	ns
t$_{PLZ}$	Output Disable Time	5.0	1.5	11.0	ns

Note 10: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V$_{CC}$ (V) (Note 11)	54ACT T$_A$ = −55°C to +125°C C$_L$ = 50 pF Guaranteed Minimum	Units	Fig. No.
t$_s$	Setup Time, HIGH or LOW D$_n$ to CP	5.0	5.5	ns	
t$_h$	Hold Time, HIGH or LOW D$_n$ to CP	5.0	1.5	ns	
t$_w$	CP Pulse Width, HIGH or LOW	5.0	5.0	ns	

Note 11: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C$_{IN}$	Input Capacitance	4.5	pF	V$_{CC}$ = OPEN
C$_{PD}$	Power Dissipation Capacitance	40	pF	V$_{CC}$ = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

0.350 ± 0.008
(8.890 ± 0.203)

0.063 − 0.075
(1.600 − 1.905)

DETAIL A

Top View

Side View

0.200 ± 0.005
(5.080 ± 0.127)
TYP

45° × 0.015 ± 0.010
(0.381 ± 0.254)

0.015
(0.381)
MIN TYP

0.007 − 0.011
(0.178 − 0.279)
R TYP

0.022 − 0.028
(0.559 − 0.711)
TYP

0.077 − 0.093
(1.959 − 2.362)

PIN # 1
INDEX

0.045 − 0.055
(1.143 − 1.397)
TYP

0.067 − 0.083
(1.702 − 2.108)
TYP

0.045 − 0.055
(1.143 − 1.397)
TYP

45° × 0.040 ± 0.010
(1.016 ± 0.254)
3 PLCS

Bottom View

0.003
(0.076)
MIN TYP

0.015
(0.381)
MAX TYP

0.022
(0.559)
MAX TYP

0.006
(0.152)
MIN TYP

Detail A

E20A (REV D)

20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

0.985
(25.019)
MAX

0.025
(0.635)
RAD

| 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 |

0.220 − 0.310
(5.588 − 7.874)

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |

0.005 − 0.020
(0.127 − 0.508)
RAD TYP

0.037 ± 0.005
(0.940 ± 0.127)

0.005
(0.127)
MIN

0.055 ± 0.005
(1.397 ± 0.127)

0.020 − 0.060
(0.508 − 1.524)

0.180
(4.572)
MAX

0.290 − 0.320
(7.366 − 8.128)

GLASS SEALANT

0.200
(5.080)
MAX

95° ± 5°

0.008 − 0.012
(0.203 − 0.305)

86° 94°

0.150
(3.810)
MIN

0.125 − 0.200
(3.175 − 5.080)

0.310 − 0.410
(7.874 − 10.41)

0.060
(1.524)
MAX
BOTH ENDS

0.018 ± 0.003
(0.457 ± 0.076)

0.100 ± 0.010
(2.540 ± 0.254)

J20A (REV M)

20 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

www.national.com

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.090
0.060

0.040
0.030
TYP

0.006
0.004
TYP

0.540 MAX

0.050 ± 0.005
TYP

20   11

0.005 MIN TYP

0.370
0.250

0.285 MAX
GLASS

0.270
0.260

0.370
0.250

DETAIL A

PIN #1
IDENT

1   10

0.019
0.015
TYP

0.045 MAX
TYP

0.012
0.008

DETAIL A

W20A (REV E)
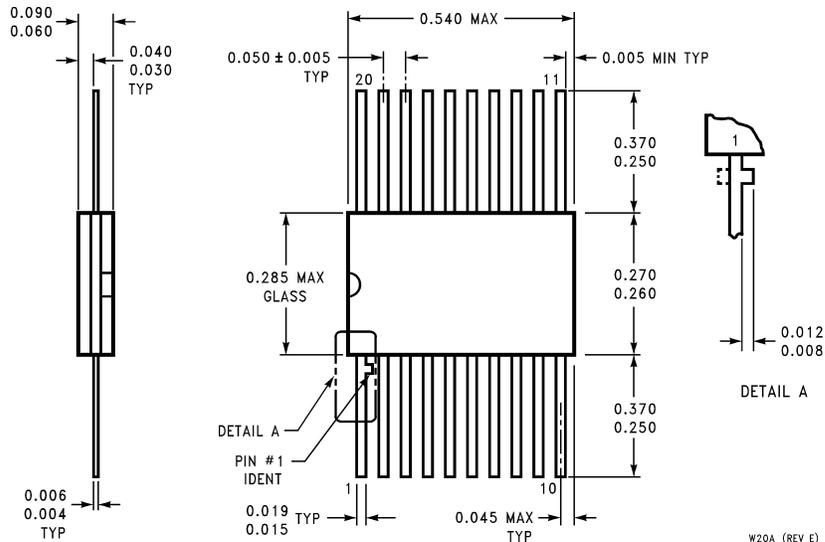
20 Lead Ceramic Flatpak (F)
NS Package Number W20A

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