

54AC258,54ACT258

54AC258 54ACT258 Quad 2-Input Multiplexer with TRI-STATE Outputs



Literature Number: SNOS103

54AC258 • 54ACT258 Quad 2-Input Multiplexer with TRI-STATE® Outputs

General Description

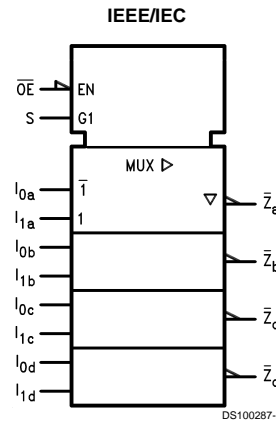
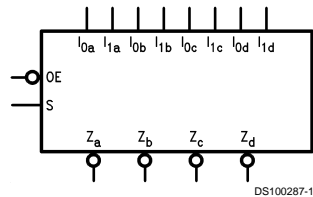
The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (\overline{OE}) input, allowing the outputs to interface directly with bus-oriented systems.

- Multiplexer expansion by tying outputs together
- Inverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT258 has TTL-compatible inputs
- Standard Military Drawing (SMD)
 - 'ACT258: 5962-88704
 - 'AC258: 5962-91604

Features

- I_{CC} and I_{OZ} reduced by 50%

Logic Symbols

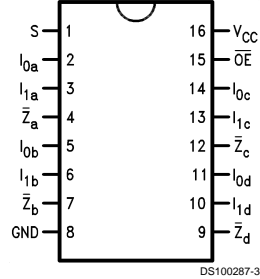


Pin Names	Description
S	Common Data Select Input
\overline{OE}	TRI-STATE Output Enable Input
I_{0a} – I_{0d}	Data Inputs from Source 0
I_{1a} – I_{1d}	Data Inputs from Source 1
\overline{Z}_a – \overline{Z}_d	TRI-STATE Inverting Data Outputs

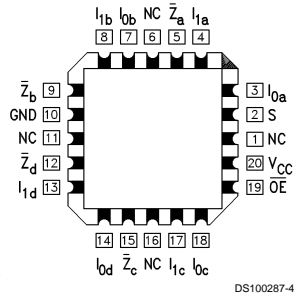
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Connection Diagrams

Pin Assignment
for DIP and Flatpak



Pin Assignment
for LCC



Functional Description

The 'AC/ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'AC/ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\bar{Z}_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$\bar{Z}_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$\bar{Z}_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$\bar{Z}_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

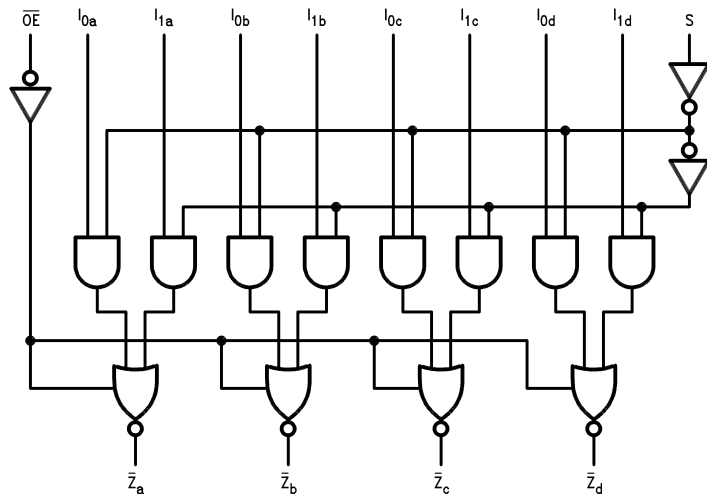
When the Output Enable input (\overline{OE}) is HIGH, the outputs are forced to a high impedance state. If the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
		I_0	I_1	
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



DS100287-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC		Units	Conditions
			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$			
			Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	3.15			
		5.5	3.85			
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	1.35			
		5.5	1.65			
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.4			
		5.5	5.4			
V_{OL}	Maximum Low Level Output Voltage	3.0	2.4	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$	
		4.5	3.7			
		5.5	4.7			
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.1			
		5.5	0.1			
V_{OL}	Maximum Low Level Output Voltage	3.0	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	
		4.5	0.50			
		5.5	0.50			
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, GND$	
I_{OZ}	Maximum TRI-STATE Current	5.5	±5.0	μA	$V_I (OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}, GND$ $V_O = V_{CC}, GND$	

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	54AC		Units	Conditions
			T _A = -55°C to +125°C			
			Guaranteed Limits			
I _{OLD}	Minimum Dynamic	5.5	50		mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 3)	5.5	-50		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0		μA	V _{IN} = V _{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	54ACT		Units	Conditions
			T _A = -55°C to +125°C			
			Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5	2.0		V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	0.8		V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.4		V	I _{OUT} = -50 μA
		5.5	5.4			
		4.5	3.70		V	(Note 5) V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA
		5.5	4.70			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.1		V	I _{OUT} = 50 μA
		5.5	0.1			
		4.5	0.50		V	(Note 5) V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA
		5.5	0.50			
I _{IN}	Maximum Input Leakage Current	5.5	±1.0		μA	V _I = V _{CC} , GND
I _{OZ}	Maximum TRI-STATE Current	5.5	±5.0		μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	1.6		mA	V _I = V _{CC} - 2.1V
I _{OLD}	Minimum Dynamic	5.5	50		mA	V _{OLD} = 1.65V Max
I _{OHD}	Output Current (Note 6)	5.5	-50		mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0		μA	V _{IN} = V _{CC} or GND

Note 5: All outputs loaded; thresholds on input associated with output under test.

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

Note 7: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 8)	54AC		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Min	Max		
t _{PLH}	Propagation Delay I _n to \bar{Z}_n	3.3	1.0	12.0	ns	
		5.0	1.0	9.5		
t _{PHL}	Propagation Delay I _n to \bar{Z}_n	3.3	1.0	10.5	ns	
		5.0	1.0	7.5		
t _{PLH}	Propagation Delay S to \bar{Z}_n	3.3	1.0	15.0	ns	
		5.0	1.0	11.5		
t _{PHL}	Propagation Delay S to \bar{Z}_n	3.3	1.0	14.0	ns	
		5.0	1.0	10.5		
t _{PZH}	Output Enable Time	3.3	1.0	11.5	ns	
		5.0	1.0	9.0		
t _{PZL}	Output Enable Time	3.3	1.0	10.5	ns	
		5.0	1.0	8.5		
t _{PHZ}	Output Disable Time	3.3	1.0	11.5	ns	
		5.0	1.0	9.5		
t _{PLZ}	Output Disable Time	3.3	1.0	10.5	ns	
		5.0	1.0	8.5		

Note 8: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

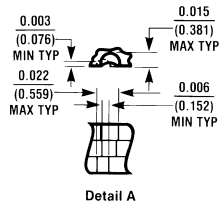
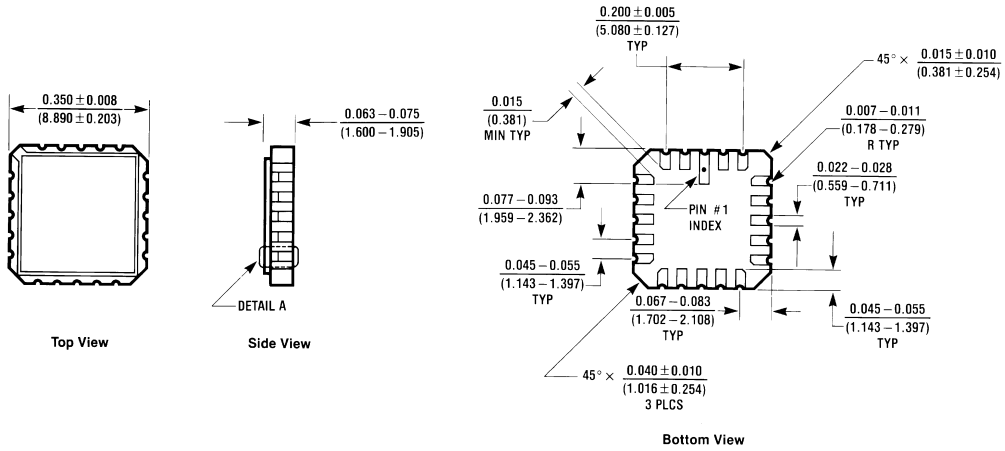
Symbol	Parameter	V _{CC} (V) (Note 9)	54ACT		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Min	Max		
t _{PLH}	Propagation Delay I _n to \bar{Z}_n	5.0	1.0	10.5	ns	
t _{PHL}	Propagation Delay I _n to \bar{Z}_n	5.0	1.0	9.0	ns	
t _{PLH}	Propagation Delay S to \bar{Z}_n	5.0	1.0	13.0	ns	
t _{PHL}	Propagation Delay S to \bar{Z}_n	5.0	1.0	12.0	ns	
t _{PZH}	Output Enable Time	5.0	1.0	10.5	ns	
t _{PZL}	Output Enable Time	5.0	1.0	10.0	ns	
t _{PHZ}	Output Disable Time	5.0	1.0	10.5	ns	
t _{PLZ}	Output Disable Time	5.0	1.0	10.0	ns	

Note 9: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

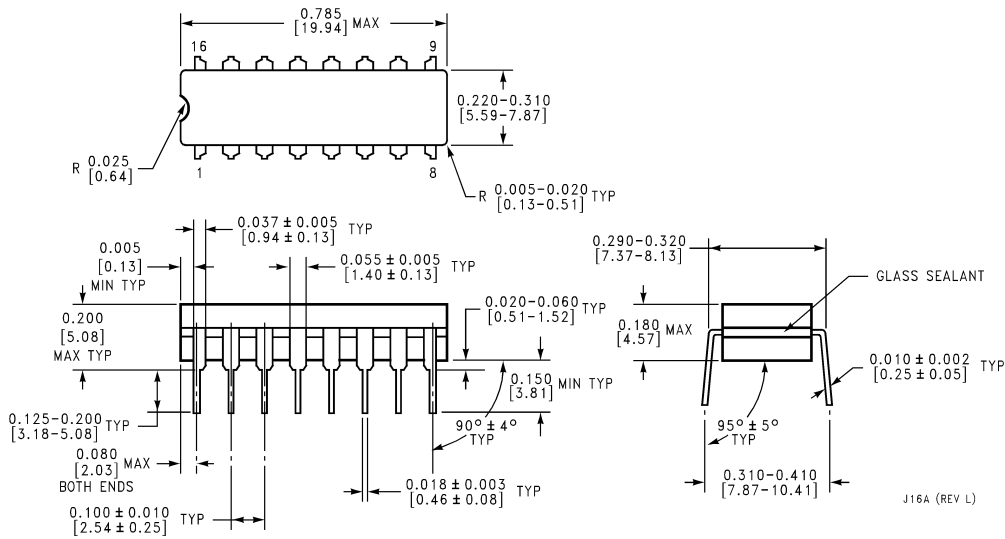
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	55.0	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

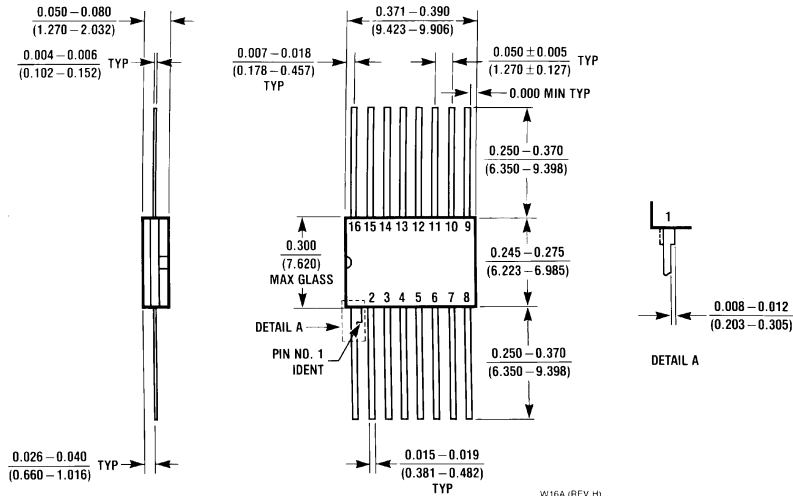
E20A (REV D)



16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

J16A (REV L)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Ceramic Flatpak (F)
NS Package Number W16A**

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