54ABT377

54ABT377 Octal D-Type Flip-Flop with Clock Enable

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National *Semiconductor*

54ABT377
Octal D-Type Flip-Flop with Clock Enable

General Description

The 'ABT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

■ Clock enable for address and data synchronization applications

■ Eight edge-triggered D flip-flops
■ Buffered common clock
■ See 'ABT273 for master reset version
■ See 'ABT373 for transparent latch version
■ See 'ABT374 for TRI-STATE® version
■ Output sink capability of 48 mA, source capability of 24 mA
■ Guaranteed latchup protection
■ High impedance glitch free bus loading during entire power up and power down cycle
■ Non-destructive hot insertion capability
■ Disable time less than enable time to avoid bus contention
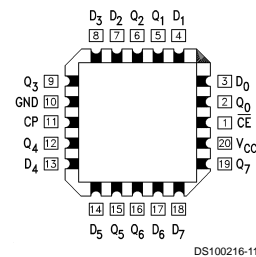■ Standard Microcircuit Drawing (SMD) 5962-9314801

Ordering Code:

Military	Package Number	Package Description
54ABT377J-QML	J20A	20-Lead Ceramic Dual-In-Line
54ABT377W-QML	W20A	20-Lead Cerpack
54ABT377E-QML	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagram

Pin Assignment for DIP and Cerpack

DS100216-1
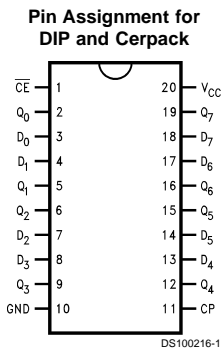
Pin Assignment for LCC

DS100216-11

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

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Truth Table

Mode Select-Function Table

Operating Mode	Inputs			Output
	CP	$\overline{CE}$	D_n	Q_n
Load "1"		l	h	H
Load "0"		l	l	L
Hold		h	X	No Change
(Do Nothing)	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
 = LOW-to-HIGH Clock Transition

Logic Diagram

DS100216-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to +4.75V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the rated I_{OL} (mA)

DC Latchup Source Current	−500 mA
(Across Comm Operating Range)	
Over Voltage Latchup	V_{CC} + 4.5V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	($\Delta V/\Delta t$)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT377			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54ABT	2.5			V	Min	I_{OH} = −3 mA
		54ABT	2.0					I_{OH} = −24 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
I_{IH}	Input HIGH Current				5	µA	Max	V_{IN} = 2.7V (Note 4)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	µA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	µA	Max	V_{IN} = 0.5V (Note 4)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA
								All Other Pins Grounded
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
I_{CCH}	Power Supply Current				50	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCT}	Maximum I_{CC}/Input Outputs Enabled							V_I = V_{CC} − 2.1V
					1.5	mA	Max	Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} No Load				0.3	mA/	Max	Outputs Open (Note 3)
						MHz		One bit Toggling, 50% Duty Cycle

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Note 3: For 8 bits toggling, I_{CCD} < 0.5 mA/MHz.

Note 4: Guaranteed but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT		Units
		T_A = −55˚C to +125˚C V_{CC} = 4.5V to 5.5V C_L = 50 pF		
		Min	Max	
f_{max}	Max Clock Frequency	150		MHz
t_{PLH}	Propagation Delay	2.2	6.0	ns
t_{PHL}	CP to O_n	2.8	6.8	

AC Operating Requirements

Symbol	Parameter	54ABT		Units
		T_A = −55˚C to +125˚C V_{CC} = 4.5V to 5.5V C_L = 50 pF		
		Min	Max	
$t_s(H)$	Setup Time, HIGH	2.0		ns
$t_s(L)$	or LOW D_n to CP	2.0		
$t_h(H)$	Hold Time, HIGH	1.8		ns
$t_h(L)$	or LOW D_n to CP	1.8		
$t_s(H)$	Setup Time, HIGH	3.0		ns
$t_s(L)$	or LOW $\overline{CE}$ to CP	3.0		
$t_h(H)$	Hold Time, HIGH	1.0		ns
$t_h(L)$	or LOW $\overline{CE}$ to CP	1.0		
$t_w(H)$	Pulse Width, CP,	3.3		ns
$t_w(L)$	HIGH or LOW	3.3		

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5	pF	V_{CC} = 0V, T_A = 25˚C
C_{OUT} (Note 5)	Output Capacitance	9	pF	V_{CC} = 5.0V

Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading
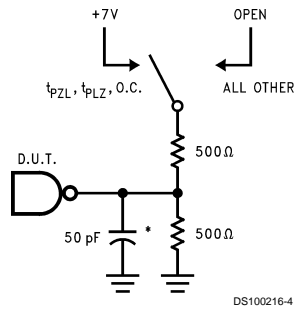
*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load
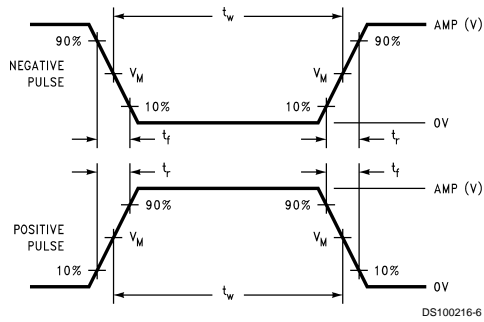
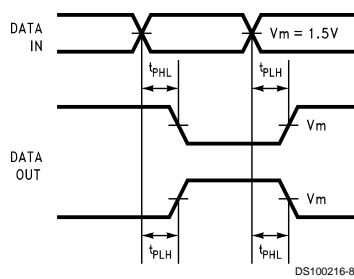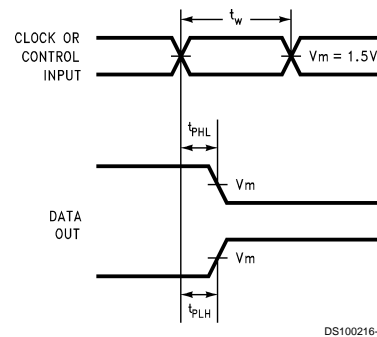**FIGURE 2. $V_M = 1.5V$**

Input Pulse Requirements

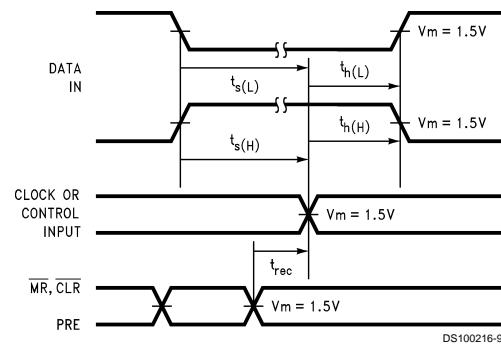| Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

**FIGURE 4. Propagation Delay Waveforms for
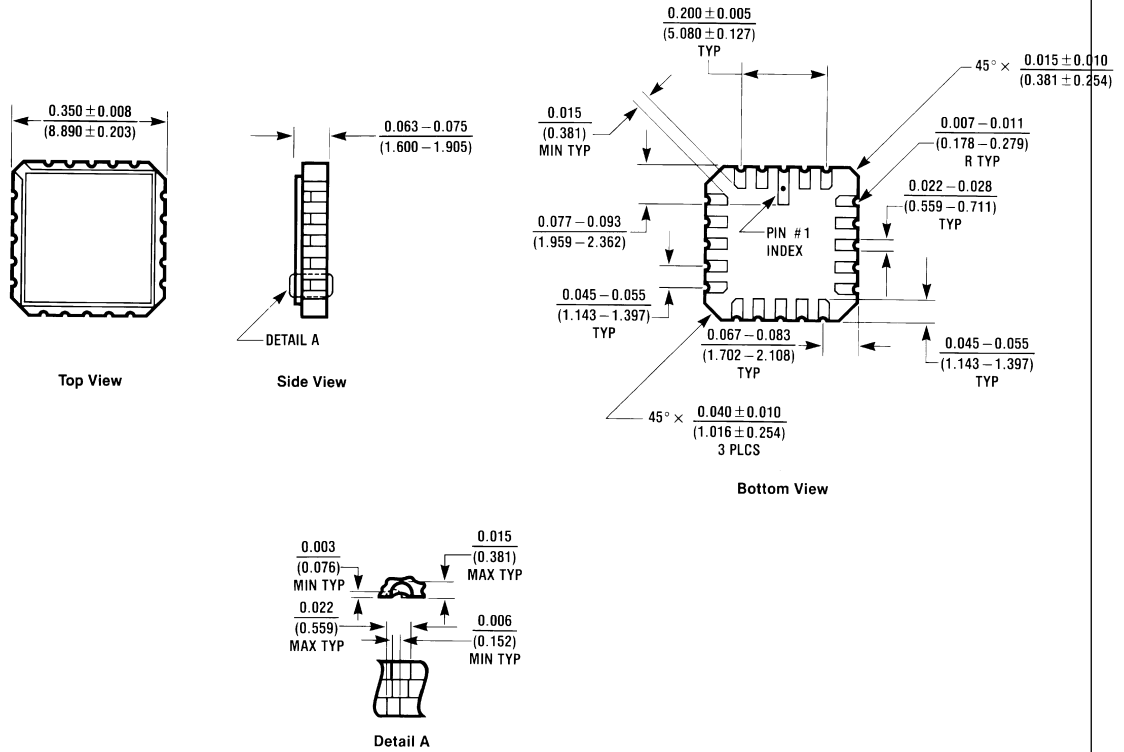Inverting and Non-Inverting Functions**

**FIGURE 5. Propagation Delay,
Pulse Width Waveforms**

**FIGURE 6. Setup Time, Hold Time
and Recovery Time Waveforms**

Physical Dimensions inches (millimeters) unless otherwise noted

0.350 ± 0.008
(8.890 ± 0.203)

0.063 − 0.075
(1.600 − 1.905)

DETAIL A

Top View

Side View

0.200 ± 0.005
(5.080 ± 0.127)
TYP

45° × 0.015 ± 0.010
(0.381 ± 0.254)

0.015
(0.381)
MIN TYP

0.007 − 0.011
(0.178 − 0.279)
R TYP

0.022 − 0.028
(0.559 − 0.711)
TYP

0.077 − 0.093
(1.959 − 2.362)

PIN #1
INDEX

0.045 − 0.055
(1.143 − 1.397)
TYP

0.067 − 0.083
(1.702 − 2.108)
TYP

0.045 − 0.055
(1.143 − 1.397)
TYP

45° × 0.040 ± 0.010
(1.016 ± 0.254)
3 PLCS

Bottom View

0.003
(0.076)
MIN TYP

0.015
(0.381)
MAX TYP

0.022
(0.559)
MAX TYP

0.006
(0.152)
MIN TYP

Detail A

E20A (REV D)

20-Lead Ceramic Chip Carrier
NS Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
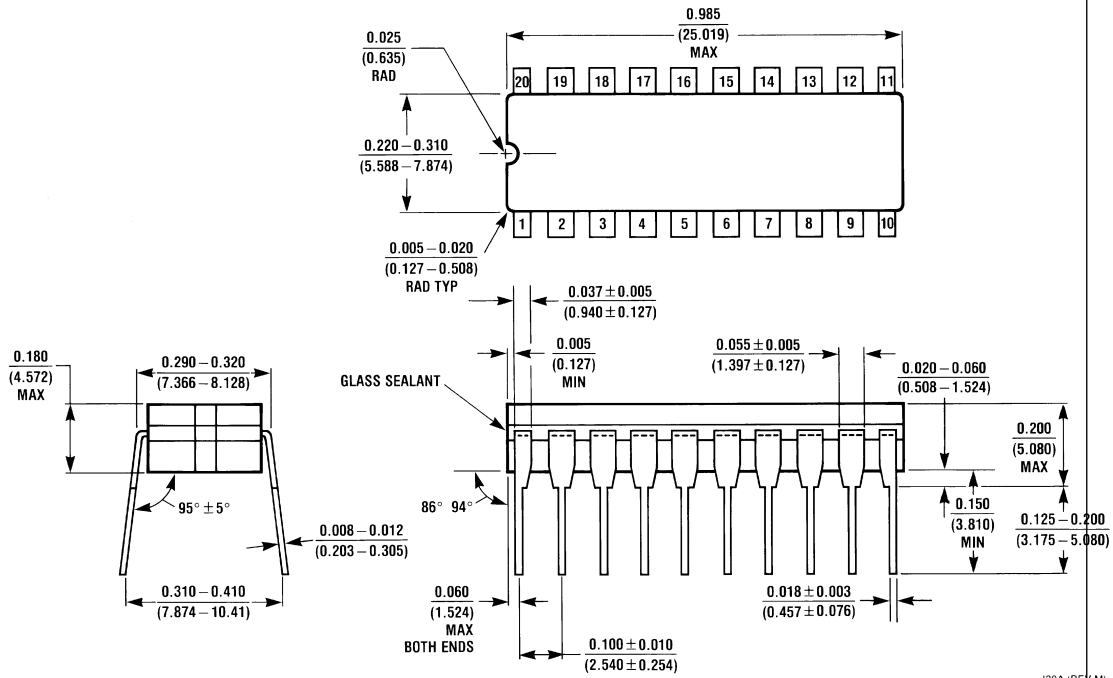
20-Lead Ceramic Dual-In-Line Package
NS Package Number J20A

J20A (REV M)
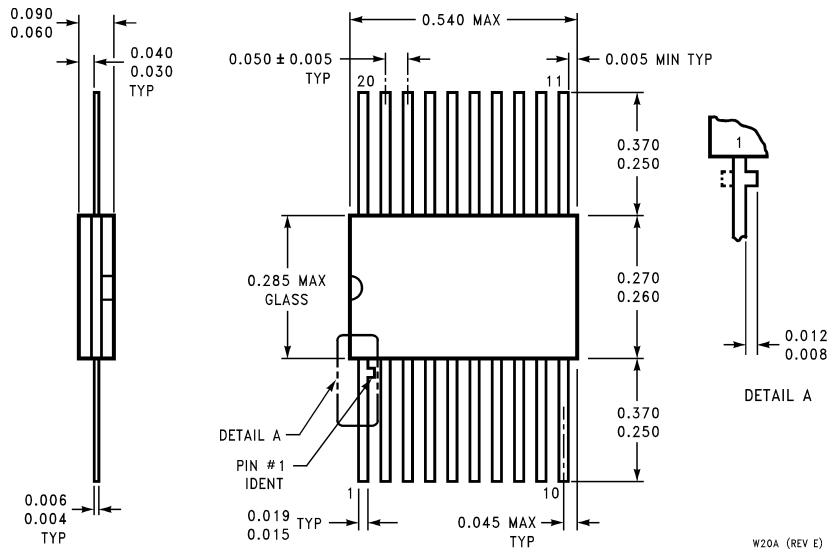
20-Lead Ceramic Flatpack
NS Package Number W20A

W20A (REV E)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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