National Semiconductor

July 1998

54ABT374
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'ABT374 is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

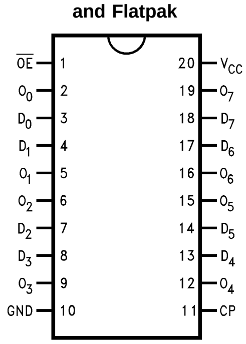
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 48 mA, source capability of 24 mA
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Standard Microcircuit Drawing (SMD) 5962-9314901

Ordering Code

Military	Package Number	Package Description
54ABT374J/883	J20A	20-Lead Ceramic Dual-In-Line
54ABT374W/883	W20A	20-Lead Cerpack
54ABT374E/883	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Connection Diagrams

Pin Assignment for DIP and Flatpak



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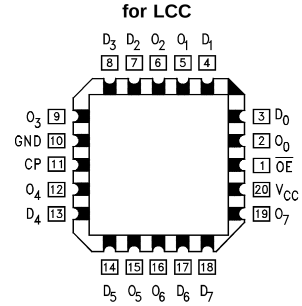
Pin Assignment for LCC



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TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Outputs

Functional Description

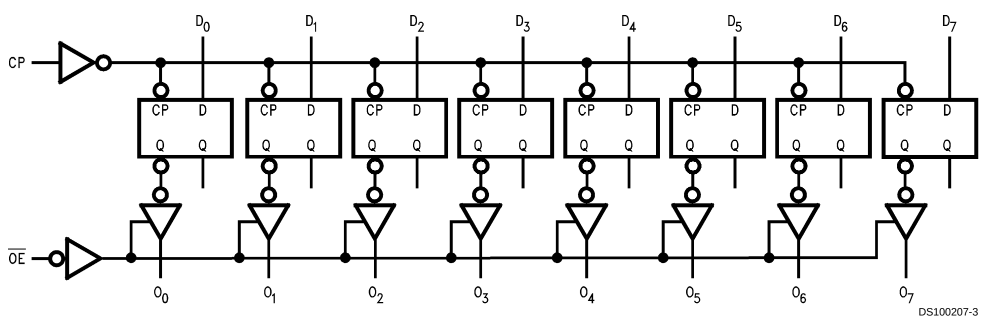
The 'ABT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to	
Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current:	
$\overline{OE}$ Pin	−150 mA
(Across Comm Operating Range)	
Other Pins	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		ABT374 Min	ABT374 Typ	ABT374 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH	54ABT	2.5			V	Min	I_{OH} = −3 mA
	Voltage	54ABT	2.0			V	Min	I_{OH} = −24 mA
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA
I_{IH}	Input HIGH Current				5	µA	Max	V_{IN} = 2.7V (Note 4)
					5			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	µA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5	µA	Max	V_{IN} = 0.5V (Note 4)
					−5			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	µA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−50	µA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	µA	0.0	V_{OUT} = 5.5V; All Others V_{CC} or GND
I_{CCH}	Power Supply Current				50	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	µA	Max	$\overline{OE}$ = V_{CC}; All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA		V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA	Max	Enable Input V_I = V_{CC} − 2.1V
		Outputs TRI-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND

DC Electrical Characteristics (Continued)

Symbol	Parameter		ABT374 Min	ABT374 Typ	ABT374 Max	Units	V_{CC}	Conditions
I_{CCD}	Dynamic I_{CC} (Note 4)	No Load			0.30	mA/ MHz	Max	Outputs Open $\overline{OE}$ = GND, (Note 3) One Bit Toggling, 50% Duty Cycle

Note 3: For 8-bit toggling, $I_{CCD} < 0.8$ mA/MHz.

Note 4: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units
		Min	Max	
f_{max}	Max Clock Frequency	150		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	1.4 2.0	6.6 7.6	ns
t_{PZH} t_{PZL}	Output Enable Time	0.8 1.5	5.7 7.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time	1.3 1.0	7.2 7.0	ns

AC Operating Requirements

Symbol	Parameter	54ABT $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units
		Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	2.5 2.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	2.5 2.5		ns
$t_w(H)$ $t_w(L)$	Pulse Width, CP HIGH or LOW	3.3 3.3		ns

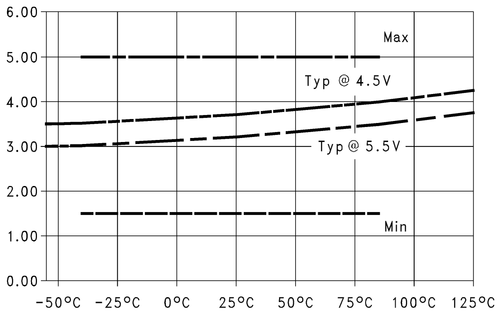
Capacitance

Symbol	Parameter	Typ	Units	Conditions ($T_A = 25°C$)
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 5)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

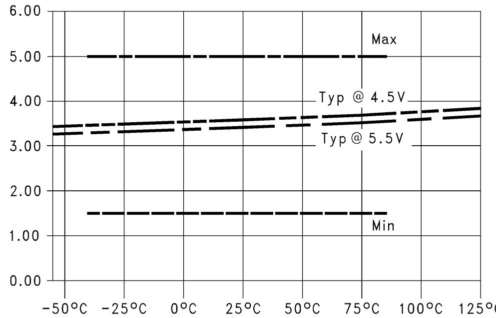
Capacitance (Continued)

t_{PLH} vs Temperature (T_A) C_L = 50 pF, 1Output Switching Clock to Output



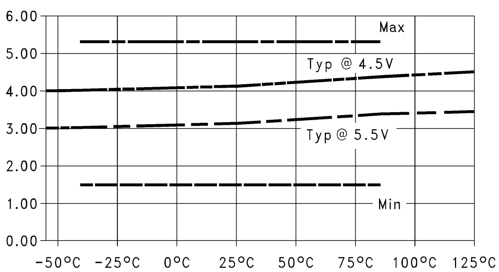
DS100207-12

t_{PHL} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching Clock to Output



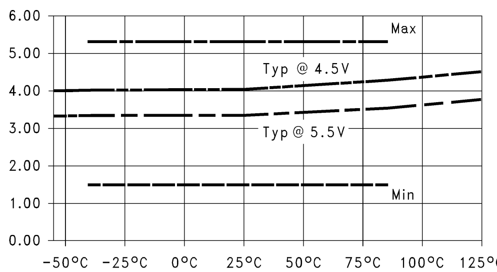
DS100207-13

t_{PZH} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching OE to Output



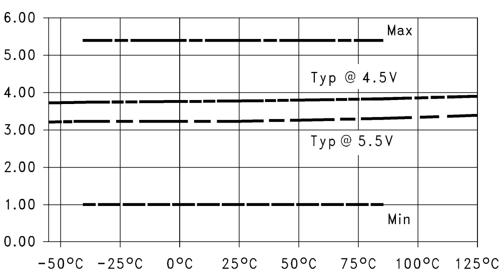
DS100207-14

t_{PZL} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching OE to Output



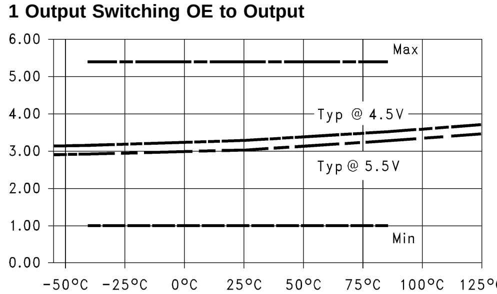
DS100207-15

t_{PHZ} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching OE to Output



DS100207-16

t_{PLZ} vs Temperature (T_A) C_L = 50 pF, 1 Output Switching OE to Output

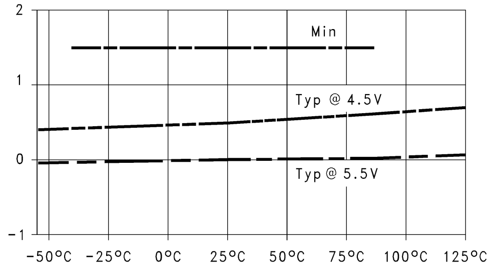


DS100207-17

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

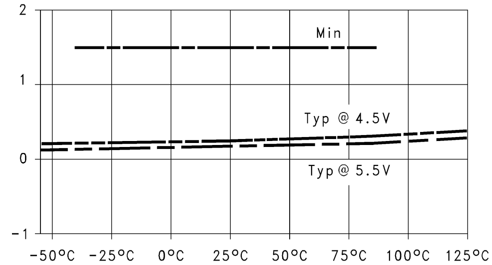
Capacitance (Continued)

t_{SET} LOW vs Temperature (T_A) C_L = 50 pF, 1 Output Switching Data to Clock



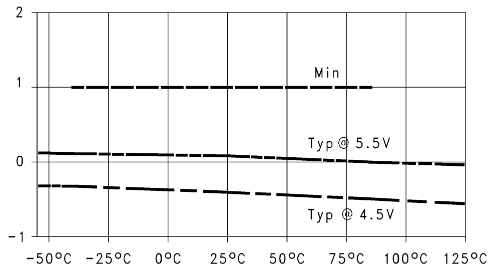
DS100207-18

t_{SET} HIGH vs Temperature (T_A) C_L = 50 pF, 1 Output Switching Data to Clock



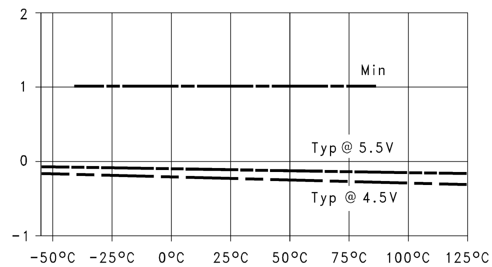
DS100207-19

t_{HOLD} HIGH vs Temperature (T_A) C_L = 50 pF, 1 Output Switching Data to Clock



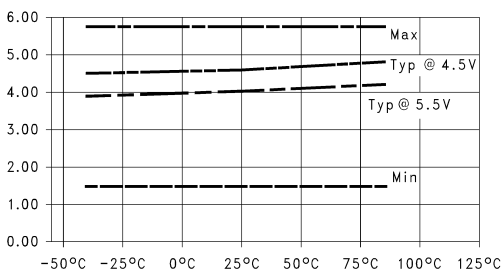
DS100207-20

t_{HOLD} LOW vs Temperature (T_A) C_L = 50 pF, 1 Output Switching Data to Clock



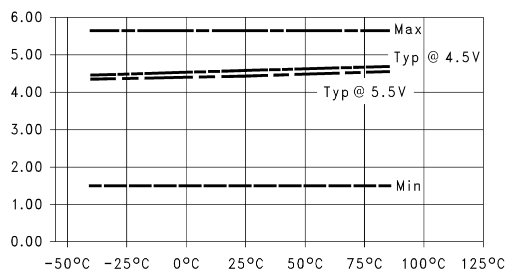
DS100207-21

t_{PLH} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching Clock to Output



DS100207-22

t_{PHL} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching Clock to Output

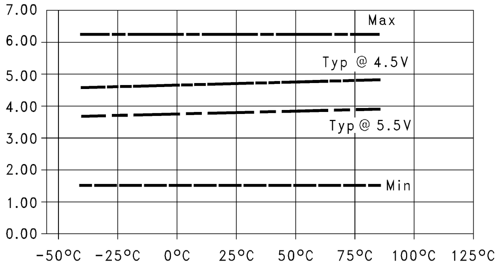


DS100207-23

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

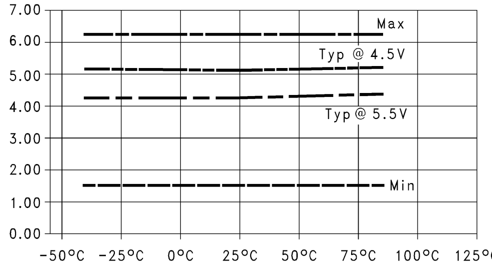
Capacitance (Continued)

t_{PZH} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching OE to Output



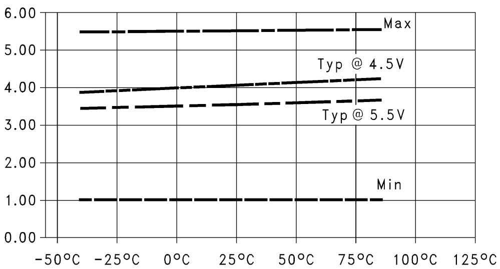
DS100207-24

t_{PZL} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching OE to Output



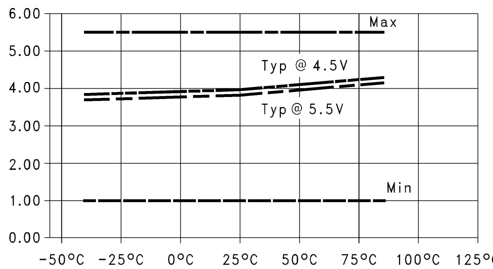
DS100207-25

t_{PHZ} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching OE to Output



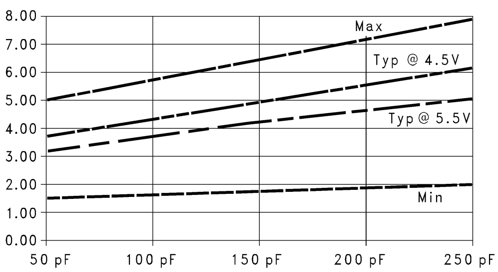
DS100207-26

t_{PLZ} vs Temperature (T_A) C_L = 50 pF, 8 Outputs Switching OE to Output



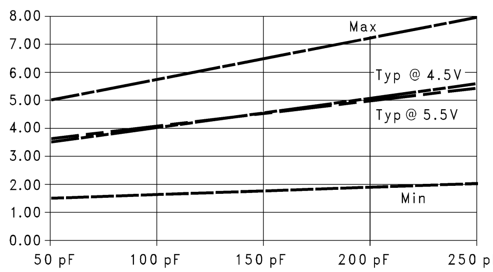
DS100207-27

t_{PLH} vs Load Capacitance T_A = 25°C, 1 Output Switching Clock to Output



DS100207-28

t_{PHL} vs Load Capacitance T_A = 25°C, 1 Output Switching Clock to Output

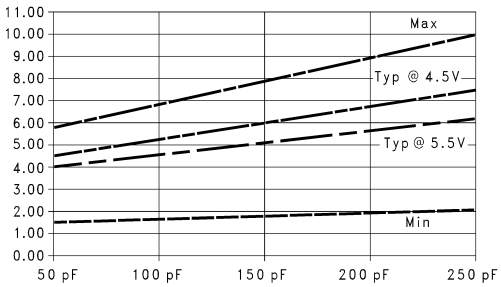


DS100207-29

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

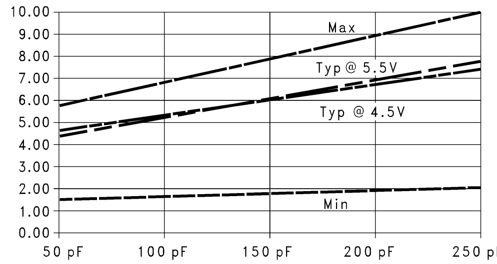
Capacitance (Continued)

t_{PLH} vs Load Capacitance T_A = 25˚C, 8 Outputs Switching Clock to Output



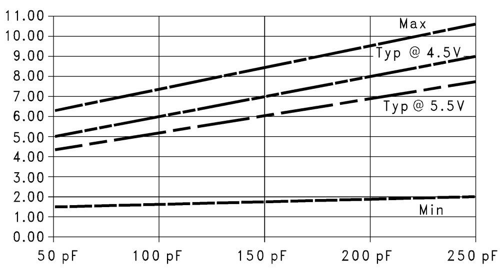
DS100207-30

t_{PHL} vs Load Capacitance T_A = 25˚C, 8 Outputs Switching Clock to Output



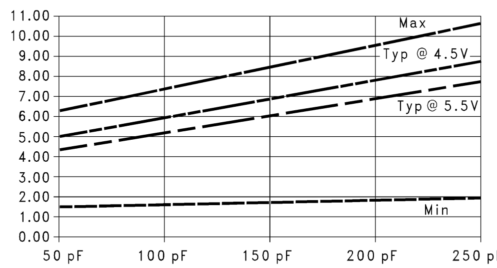
DS100207-31

t_{PZH} vs Load Capacitance T_A = 25˚C, 8 Outputs Switching $\overline{OE}$ to Output



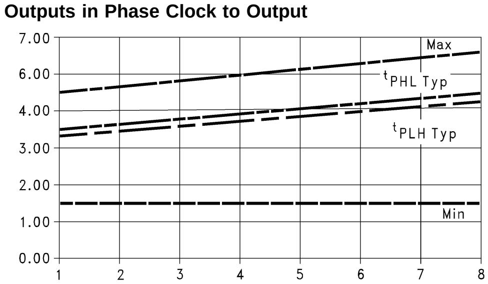
DS100207-32

t_{PZL} vs Load Capacitance T_A = 25˚C, 8 Outputs Switching $\overline{OE}$ to Output



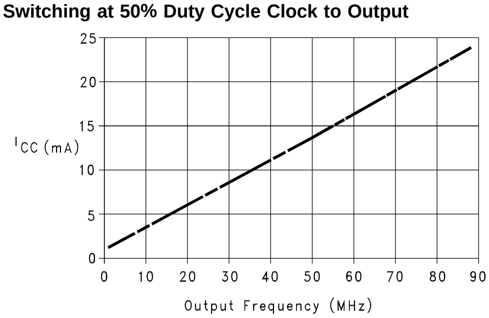
DS100207-33

t_{PLH} and t_{PHL} vs Number Outputs Switching C_L = 50 pF, T_A = 25˚C, V_{CC} = 5.0V, Outputs in Phase Clock to Output



DS100207-34

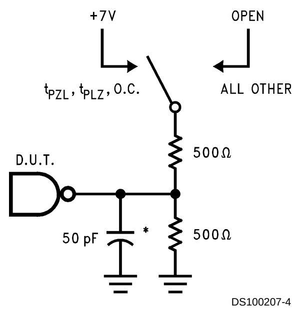
Typical I_{CC} vs Output Switching Frequency C_L = 0 pF, V_{CC} = V_{IH} = 5.5V, 1 Output Switching at 50% Duty Cycle Clock to Output



DS100207-35

Dashed lines represent design characteristics; for specified guarantees, refer to AC Characteristics Tables.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

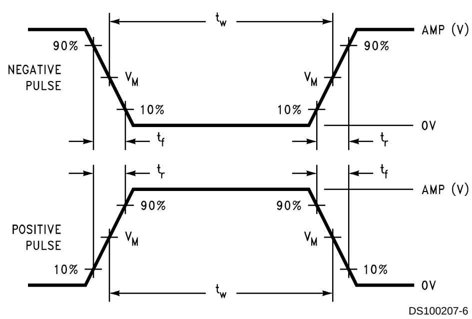


FIGURE 2. V_M = 1.5V

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

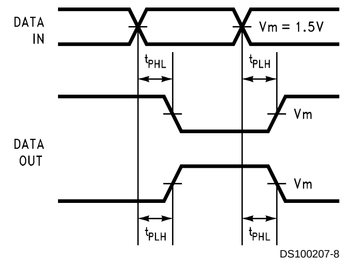


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

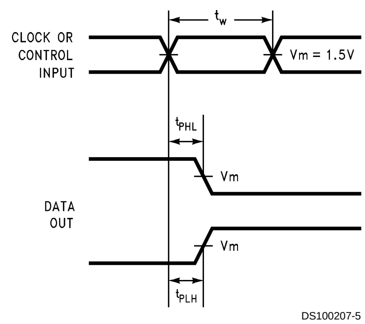


FIGURE 5. Propagation Delay, Pulse Width Waveforms

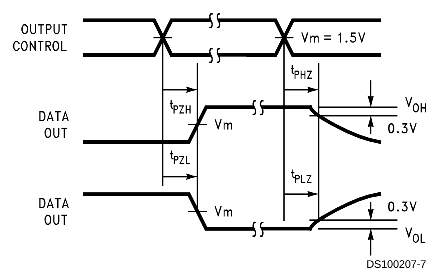


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

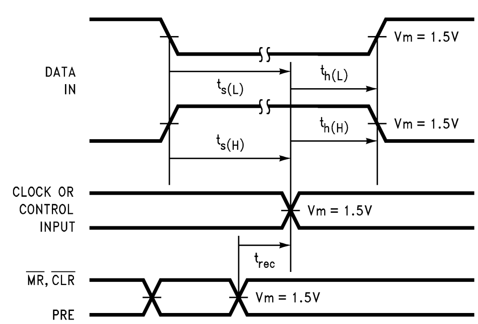
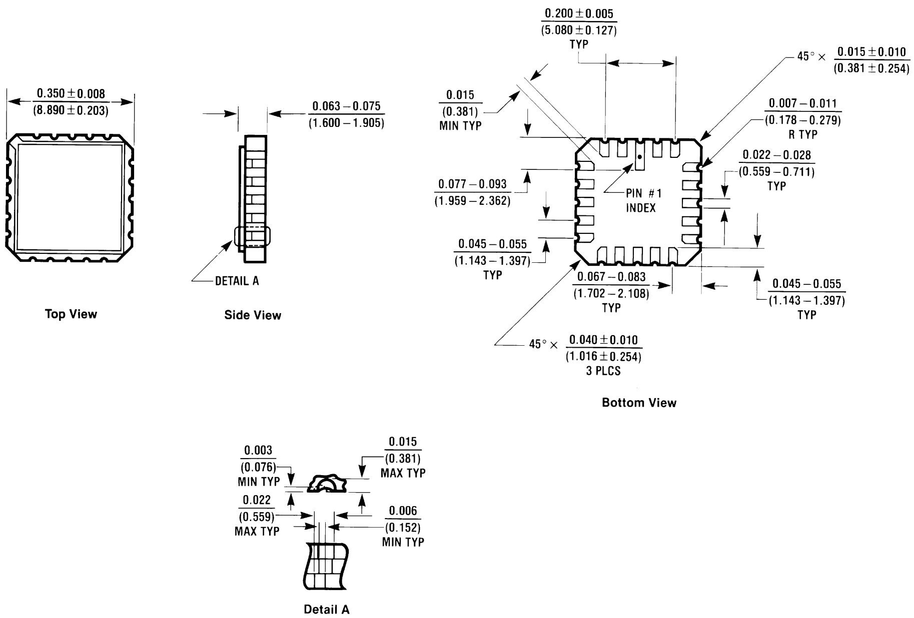
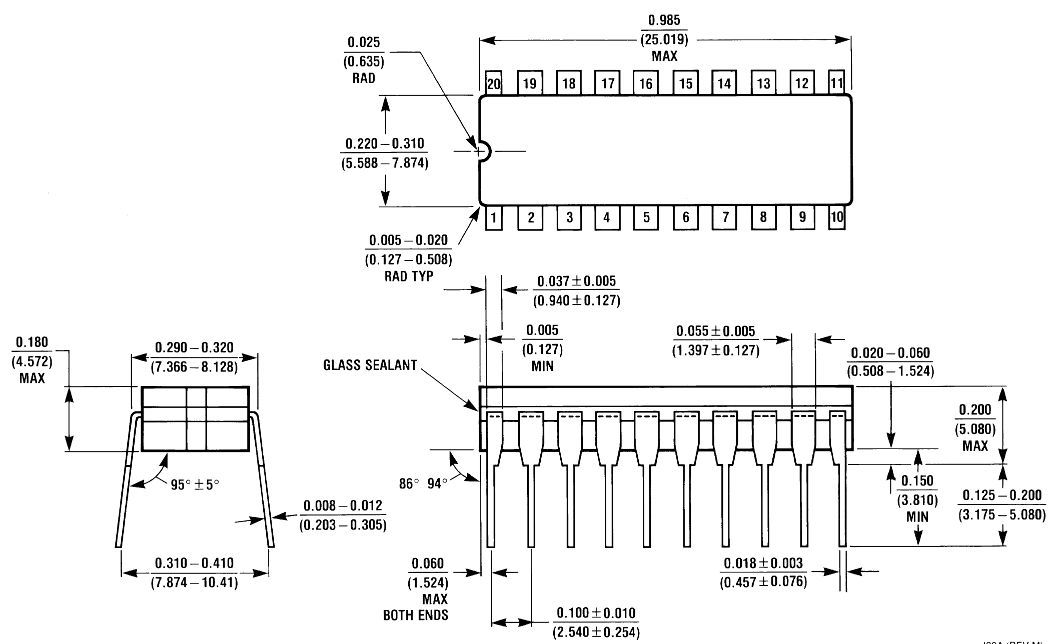


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

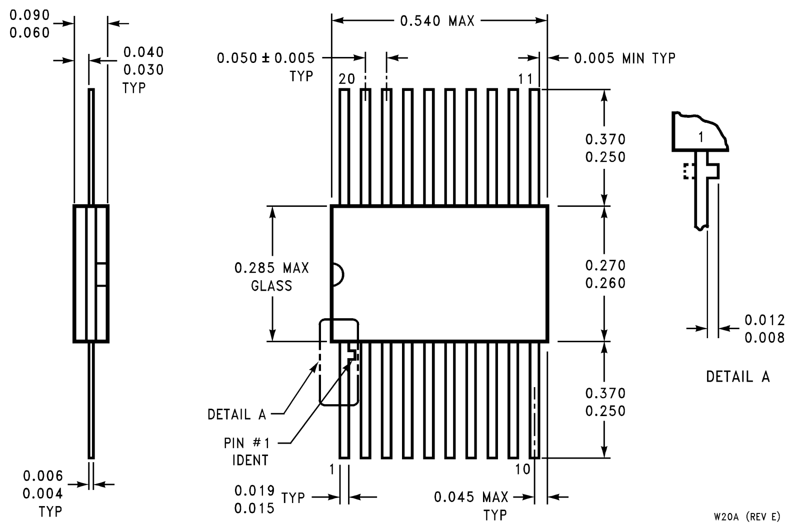


20-Terminal Ceramic Chip Carrier (L)
NS Package Number E20A



20-Lead Ceramic Dual-In-Line (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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