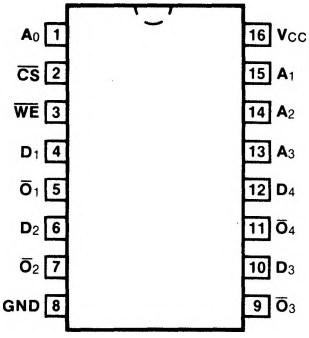
# 54/7489
# 54LS/74LS89

## 64-BIT RANDOM ACCESS MEMORY

(With Open-Collector Outputs)

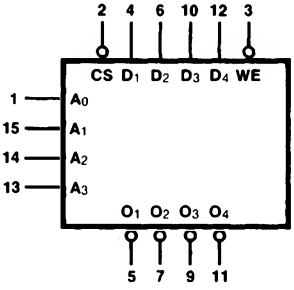
**CONNECTION DIAGRAM**
PINOUT A




**DESCRIPTION** — The '89 a high speed, low power 64-bit Random Access Memory organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state when both the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) are HIGH. For all other combinations of $\overline{CS}$ and $\overline{WE}$ the outputs are active, presenting the complement of either the stored data (READ mode) or the information present on the D inputs.

- **OPEN-COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**

**LOGIC SYMBOL**




$V_{CC}$ = Pin 16
GND = Pin 8

**ORDERING CODE:** See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE<br>$V_{CC}$ = +5.0 V ±5%,<br>$T_A$ = 0°C to +70°C | MILITARY GRADE<br>$V_{CC}$ = +5.0 V ±10%,<br>$T_A$ = -55°C to +125°C | PKG TYPE |
|---|---|---|---|---|
| Plastic DIP (P) | A | 7489PC, 74LS89PC | | 9B |
| Ceramic DIP (D) | A | 7489DC, 74LS89DC | 5489DM, 54LS89DM | 7B |
| Flatpak (F) | A | 7489FC, 74LS89FC | 5489FM, 54LS89FM | 4L |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

| PIN NAMES | DESCRIPTION | 54/74 (U.L.) HIGH/LOW | 54/74LS (U.L.) HIGH/LOW |
|---|---|---|---|
| $A_0 - A_3$ | Address Inputs | 1.0/1.0 | 0.5/0.013 |
| $\overline{CS}$ | Chip Select Input (Active LOW) | 1.0/1.0 | 0.5/0.013 |
| $\overline{WE}$ | Write Enable Input (Active LOW) | 1.0/1.0 | 0.5/0.013 |
| $D_1 - D_4$ | Data Inputs | 1.0/1.0 | 0.5/0.013 |
| $\overline{O}_1 - \overline{O}_4$ | Inverted Data Outputs | OC*/7.5 | OC*/10 (5.0) |

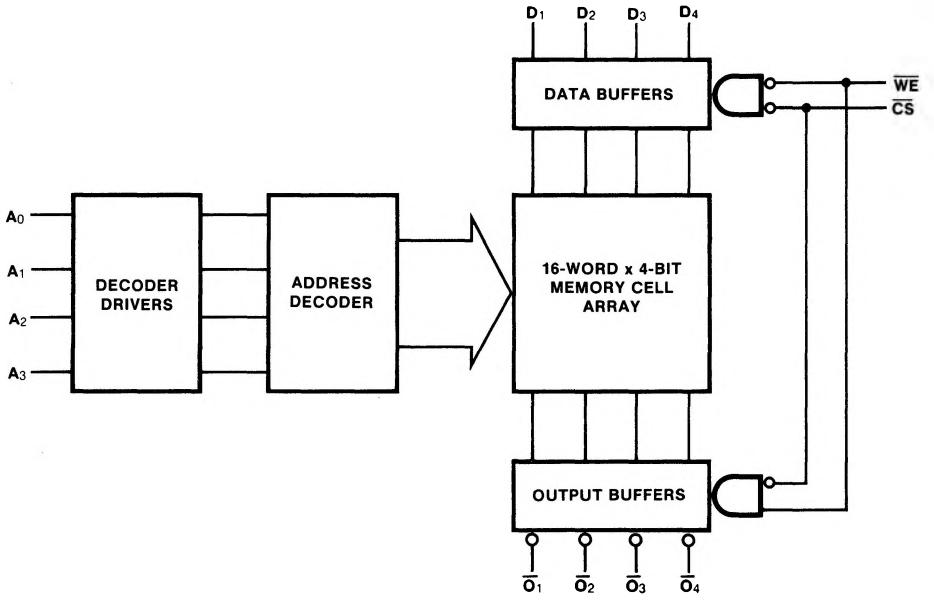
*OC — Open Collector

**FUNCTION TABLE**

| INPUTS | | OPERATION | CONDITION OF OUTPUTS |
|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | | |
| L | L | Write | Complement of Data Inputs |
| L | H | Read | Complement of Selected Word |
| H | L | Inhibit Entry | Undetermined |
| H | H | Hold | (Off) HIGH |

H = HIGH Voltage Level
L = LOW Voltage Level

**LOGIC DIAGRAM**



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | | 54/74 Min | 54/74 Max | 54/74LS Min | 54/74LS Max | UNITS | CONDITIONS | |
|---|---|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output HIGH Current | | | 20 | | 20 | μA | $V_{CC}$ = Min, $V_{OH}$ = 5.5 V | |
| $V_{OL}$ | Output LOW Voltage | | | 0.4 | | | V | $I_{OL}$ = 12 mA | $V_{CC}$ = Min |
| | | | | 0.45 | | | | $I_{OL}$ = 16 mA | |
| | | XM, XC | | | | 0.4 | V | $I_{OL}$ = 8.0 mA | $V_{CC}$ = Min |
| | | XC | | | | 0.5 | | $I_{OL}$ = 16 mA | |
| $I_{CC}$ | Power Supply Current | | | 105 | | 40 | mA | $V_{CC}$ = Min, $\overline{CS}$ = Gnd | |
| $C_O$ | Off-State Output Capacitance | | | 4.0* | | 4.0* | pF | $V_O$ = 2.4 V, f = 1 MHz | |

**AC CHARACTERISTICS:** $V_{CC}$ = +5.0 V, $T_A$ = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL | PARAMETER | 54/74 $C_L$ = 30 pF, $R_L$ = 300 Ω Min | 54/74 $C_L$ = 30 pF, $R_L$ = 300 Ω Max | 54/74LS $C_L$ = 15 pF, $R_L$ = 2 kΩ Min | 54/74LS $C_L$ = 15 pF, $R_L$ = 2 kΩ Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay | | 50 | | 10* | ns | Figs. 3-2, 3-5 |
| $t_{PHL}$ | $\overline{CS}$ to $\overline{O}_n$ | | 50 | | 10* | | '89 has 600 Ω to Gnd |
| $t_{PLH}$ | Propagation Delay | | 60 | | 37* | ns | Figs. 3-2, 3-20 |
| $t_{PHL}$ | $A_n$ to $\overline{O}_n$ | | 60 | | 37* | | '89 has 600 Ω to Gnd |
| $t_{rec}$ | Recovery Time $\overline{WE}$ to $\overline{O}_n$ | | 70 | | 30* | ns | Figs. 3-2, 3-4, 3-5 '89 has 600 Ω to Gnd |

**AC OPERATING REQUIREMENTS:** $V_{CC}$ = +5.0 V, $T_A$ = +25°C

| SYMBOL | PARAMETER | 54/74 Min | 54/74 Max | 54/74LS Min | 54/74LS Max | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| $t_s$ (H) | Setup Time HIGH or LOW | 40 | | 25* | | ns | Fig. 3-13 |
| $t_s$ (L) | $D_n$ to $\overline{WE}$ | 40 | | 25* | | | |
| $t_s$ (H) | Setup Time HIGH or LOW | 0 | | 10* | | ns | Fig. 3-21 |
| $t_s$ (L) | $A_n$ to $\overline{WE}$ | 0 | | 10* | | | |
| $t_h$ (H) | Hold Time HIGH or LOW | 5.0 | | 0* | | ns | Figs. 3-13, 3-21 |
| $t_h$ (L) | $D_n$ or $A_n$ to $\overline{WE}$ | 5.0 | | 0* | | | |
| $t_w$ (L) | $\overline{WE}$ Pulse Width LOW | 40 | | 25* | | ns | Fig. 3-21 |

*Typical Value