

**54/7474**  
**54H/74H74**  
**54S/74S74**  
**54LS/74LS74**

**DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP**

**DESCRIPTION** — The '74 devices are dual D-type flip-flops with Direct Clear and Set inputs and complementary (Q,  $\bar{Q}$ ) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

**TRUTH TABLE**  
 (Each Half)

INPUT	OUTPUTS	
@ $t_n$	@ $t_n + 1$	
D	Q	$\bar{Q}$
L	L	H
H	H	L

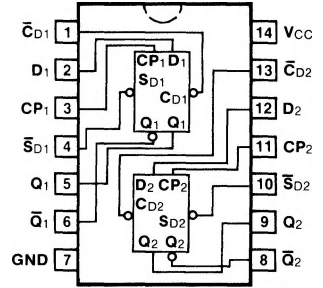
**Asynchronous Inputs:**  
 LOW input to  $\bar{S}_D$  sets Q to HIGH level  
 LOW input to  $\bar{C}_D$  sets Q to LOW level  
 Clear and Set are independent of clock  
 Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 $t_n$  = Bit time before clock pulse.  
 $t_n + 1$  = Bit time after clock pulse.

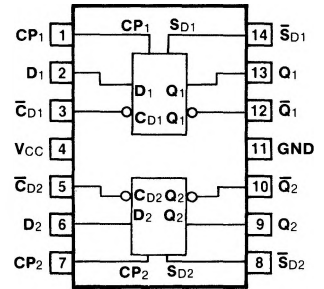
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$ , $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$ , $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	7474PC, 74H74PC 74S74PC, 74LS74PC		9A
Ceramic DIP (D)	A	7474DC, 74H74DC 74S74DC, 74LS74DC	5474DM, 54H74DM 54S74DM, 54LS74DM	6A
Flatpak (F)	A	74S74FC, 74LS74FC	54S74FM, 54LS74FM	3I
	B	7474FC, 74H74FC	5474FM, 54H74FM	

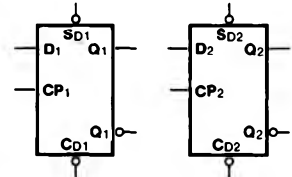
**CONNECTION DIAGRAMS**  
**PINOUT A**



**PINOUT B**



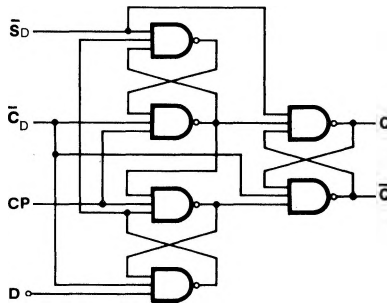
**LOGIC SYMBOL**



$V_{CC} = \text{Pin } 14 (4)$   
 $GND = \text{Pin } 7 (11)$

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
D <sub>1</sub> , D <sub>2</sub>	Data Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
CP <sub>1</sub> , CP <sub>2</sub>	Clock Pulse Inputs (Active Rising Edge)	2.0/2.0	2.5/2.5	2.5/2.5	1.0/0.5
$\bar{C}D_1$ , $\bar{C}D_2$	Direct Clear Inputs (Active LOW)	3.0/2.0	3.75/2.5	3.75/3.75	1.5/0.75
$\bar{S}D_1$ , $\bar{S}D_2$	Direct Set Inputs (Active LOW)	2.0/1.0	2.5/1.25	2.5/2.5	1.0/0.5
Q <sub>1</sub> , $\bar{Q}_1$ , Q <sub>2</sub> , $\bar{Q}_2$	Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

**LOGIC DIAGRAM** (one half shown)**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74H		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max	Min	Max		
I <sub>CC</sub>	Power Supply Current	XM	30	42	50	8.0	mA	V <sub>CC</sub> = Max, V <sub>CP</sub> = 0 V			
		XC	30	50	50	8.0					

**AC CHARACTERISTICS:** V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74H		54/74S		54/74LS		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 400 Ω		C <sub>L</sub> = 25 pF R <sub>L</sub> = 280 Ω		C <sub>L</sub> = 15 pF R <sub>L</sub> = 280 Ω		C <sub>L</sub> = 15 pF			
		Min	Max	Min	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Clock Frequency	15	35	75	30	MHz	Figs. 3-1, 3-8				
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or $\bar{Q}_n$	25 40	15 20	9.0 11	25 35	ns	Figs. 3-1, 3-8				
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\bar{C}D_n$ or $\bar{S}D_n$ to Q <sub>n</sub> or $\bar{Q}_n$	25 40	20 30	6.0 13.5	15 35	ns	V <sub>CP</sub> ≥ 2.0 V Figs. 3-1, 3-10				
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\bar{C}D_n$ or $\bar{S}D_n$ to Q <sub>n</sub> or $\bar{Q}_n$	25 40	20 30	6.0 8.0	15 24	ns	V <sub>CP</sub> ≤ 0.8 V Figs. 3-1, 3-10				

**AC OPERATING REQUIREMENTS:  $V_{CC} = +5.0\text{ V}$ ,  $T_A = +25^\circ\text{C}$** 

SYMBOL	PARAMETER	54/74		54/74H		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max	Min	Max		
$t_s$ (H)	Setup Time HIGH $D_n$ to $CP_n$	20		10		3.0		10		ns	Fig. 3-6
$t_h$ (H)	Hold Time HIGH $D_n$ to $CP_n$	5.0		0		0		5.0		ns	
$t_s$ (L)	Setup Time LOW $D_n$ to $CP_n$	20		15		3.0		20		ns	Fig. 3-6
$t_h$ (L)	Hold Time LOW $D_n$ to $CP_n$	5.0		0		0		5.0		ns	
$t_w$ (H)	$CP_n$ Pulse Width	30		15		6.0		18		ns	Fig. 3-8
$t_w$ (L)		37		13.5		7.3		15.5			
$t_w$ (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	30		25		7.0		15		ns	Fig. 3-10