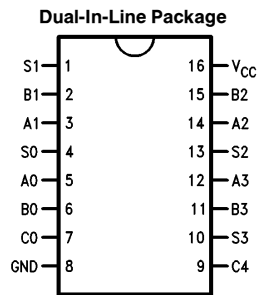


## 54283/DM74283 4-Bit Binary Full Adder (with Fast Carry)

### General Description

The '283 high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words (A0–A3, B0–B3) and a Carry input (C0). They generate the binary Sum outputs (S0–S3) and the Carry output (C4) from the most significant bit. They operate with either active HIGH or active LOW operands (positive or negative logic).

### Connection Diagram



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Order Number 54283DMQB, 54283FMQB or DM74283N  
See NS Package Number J16A, N16E or W16A

Pin Names	Description
A0–A3	A Operand Inputs
B0–B3	B Operand Inputs
C0	Carry Input
S0–S3	Sum Outputs
C4	Carry Output

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54	–55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	54283			DM74283			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8			0.8	V
I <sub>OH</sub>	High Level Output Current			–0.4			–0.4	mA
I <sub>OL</sub>	Low Level Output Current			16			16	mA
T <sub>A</sub>	Free Air Operating Temperature	–55		125	0		70	°C

## Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = –12 mA			–1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max	2.4	3.4		V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min		0.2	0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.4V			40	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			–1.6	mA
I <sub>OS</sub>	Short Circuit Output Current at S <sub>n</sub>	V <sub>CC</sub> = Max (Note 2)	54	–20	–55	mA
			DM74	–20	–55	
I <sub>OS</sub>	Short Circuit Output Current at C4	V <sub>CC</sub> = Max (Note 2)	54	–20	–70	mA
			DM74	–18	–70	
I <sub>CCH</sub>	Supply Current with Outputs High	V <sub>CC</sub> = Max	54		99	mA
			DM74		110	

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time.

## Switching Characteristics

$V_{CC} = +5.0V$ ,  $T_A = +25^\circ C$  (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$C_L = 15 \text{ pF}$ , $R_L = 400\Omega$		Units
		Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C_0$ or $S_n$		21	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ or $B_n$ to $S_n$		24	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C_0$ to $C_4$		14 16	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ or $B_n$ to $C_4$		14 16	ns

## Functional Description

The '283 adds two 4-bit binary words (A plus B) plus the incoming carry  $C_0$ . The binary sum appears on the Sum ( $S_0$ – $S_3$ ) and outgoing carry ( $C_4$ ) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus  $C_0$ ,  $A_0$ ,  $B_0$  can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the '283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that if  $C_0$  is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Example:

	$C_0$	$A_0$	$A_1$	$A_2$	$A_3$	$B_0$	$B_1$	$B_2$	$B_3$	$S_0$	$S_1$	$S_2$	$S_3$	$C_4$
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH:  $0 + 10 + 9 = 3 + 16$  Active LOW:  $1 + 5 + 6 = 12 + 0$

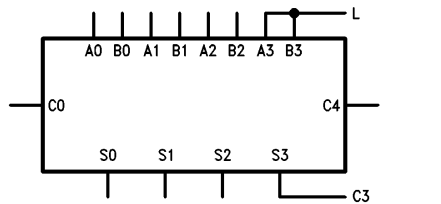


FIGURE a. 3-Bit Adder

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Due to pin limitations, the intermediate carries of the '283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. *Figure a* shows a way of making a 3-bit adder. Tying the operand inputs of the fourth adder ( $A_3$ ,  $B_3$ ) LOW makes  $S_3$  dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, *Figure b* shows a way of dividing the '283 into a 2-bit and a 1-bit adder. The third stage adder ( $A_2$ ,  $B_2$ ,  $S_2$ ) is used merely as a means of getting a carry ( $C_{10}$ ) signal into the fourth stage (via  $A_2$  and  $B_2$ ) and bringing out the carry from the second stage on  $S_2$ . Note that as long as  $A_2$  and  $B_2$  are the same, whether HIGH or LOW, they do not influence  $S_2$ . Similarly, when  $A_2$  and  $B_2$  are the same the carry into the third stage does not influence they carry out of the third stage. *Figure c* shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs  $S_0$ ,  $S_1$  and  $S_2$  present a binary number equal to the number of inputs  $I_1$ – $I_5$  that are true. *Figure d* shows one method of implementing a 5-input majority gate. When three or more of the inputs  $I_1$ – $I_5$  are true, the output  $M_5$  is true.

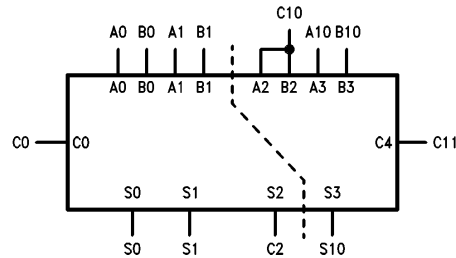


FIGURE b. 2-Bit and 1-Bit Adders

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## Functional Description (Continued)

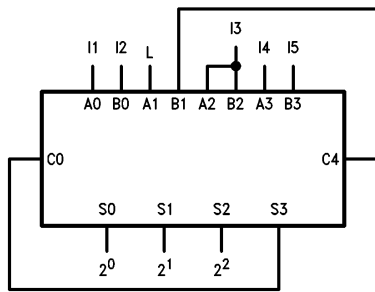


FIGURE c. 5-Input Encoder

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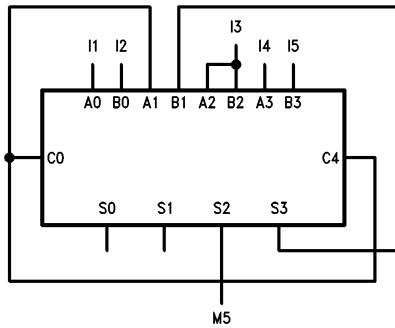
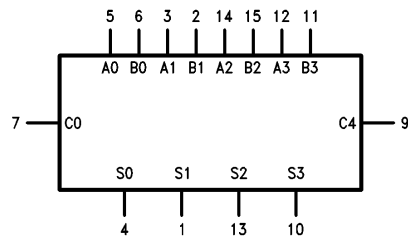


FIGURE d. 5-Input Majority Gate

TL/F/9786-6

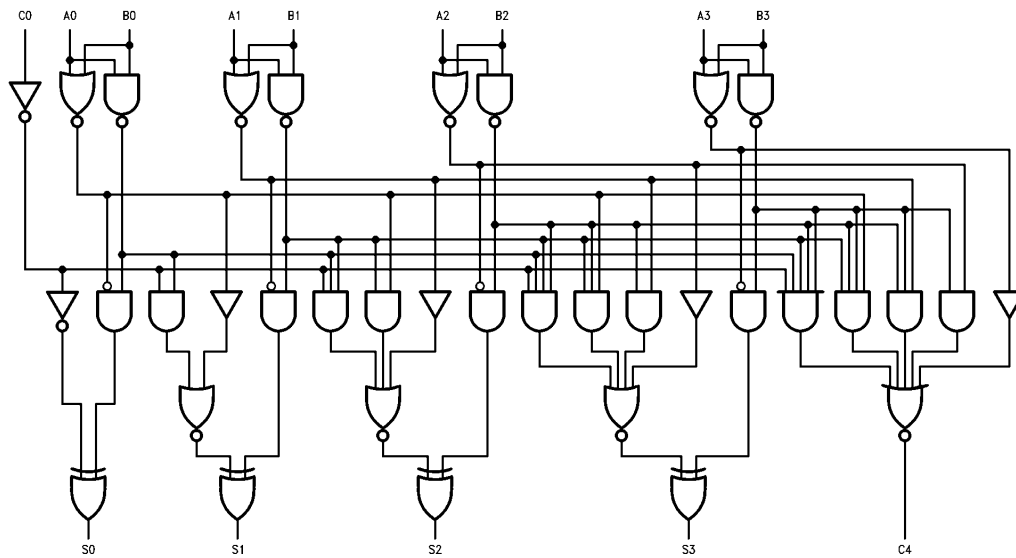
## Logic Symbol



TL/F/9786-2

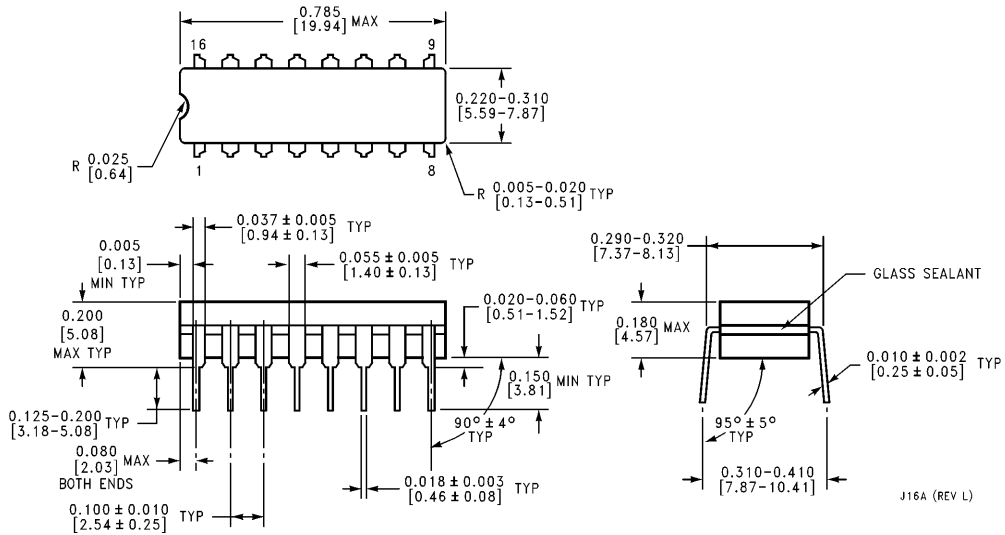
V<sub>CC</sub> = Pin 16  
GND = Pin 8

## Logic Diagram

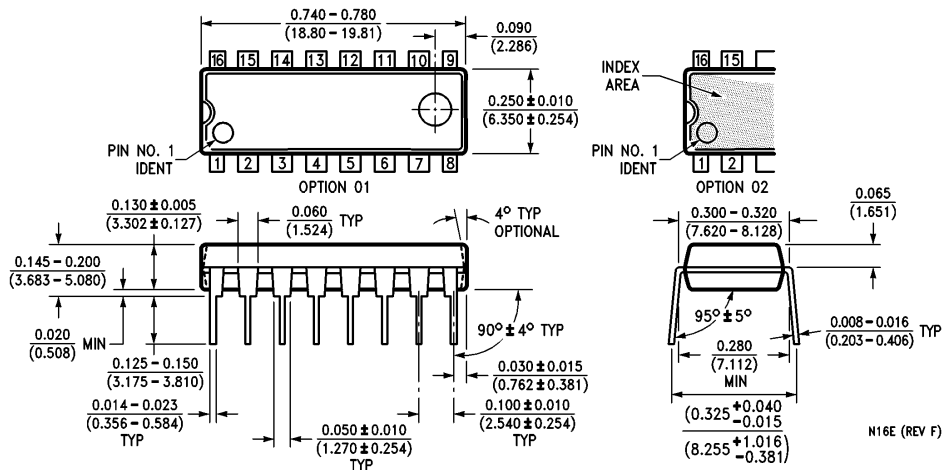


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**Physical Dimensions** inches (millimeters)

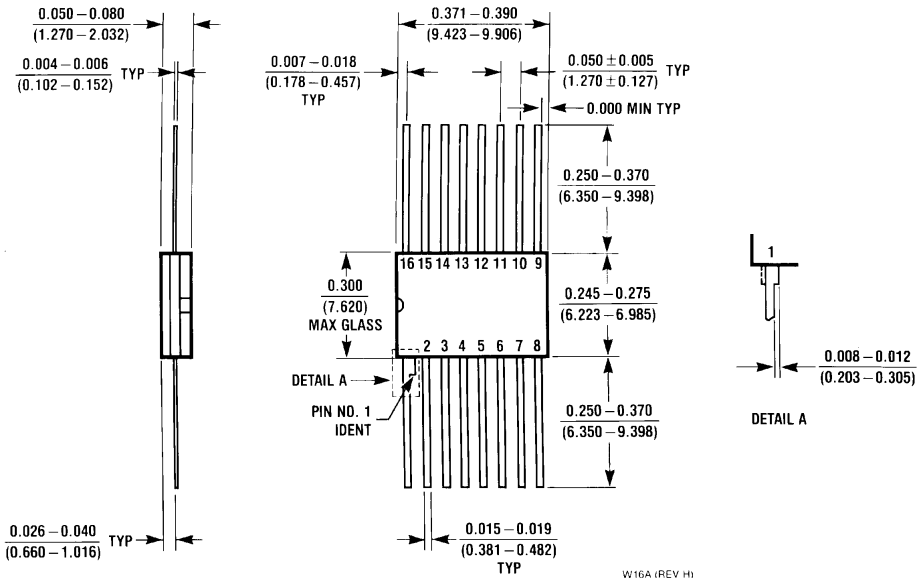


**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number 54283DMQB**  
**NS Package Number J16A**



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74283N**  
**NS Package Number N16E**

**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead Ceramic Flat Package (W)**  
**Order Number 54283FMQB**  
**NS Package Number W16A**

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**National Semiconductor Corporation**  
 1111 West Bardin Road  
 Arlington, TX 76017  
 Tel: 1(800) 272-9959  
 Fax: 1(800) 737-7018

**National Semiconductor Europe**  
 Fax: (+49) 0-180-530 85 86  
 Email: onjwge@tevm2.nsc.com  
 Deutsch Tel: (+49) 0-180-530 85 85  
 English Tel: (+49) 0-180-532 78 32  
 Français Tel: (+49) 0-180-532 93 58  
 Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
 19th Floor, Straight Block,  
 Ocean Centre, 5 Canton Rd.  
 Tsimshatsui, Kowloon  
 Hong Kong  
 Tel: (852) 2737-1600  
 Fax: (852) 2736-9960

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