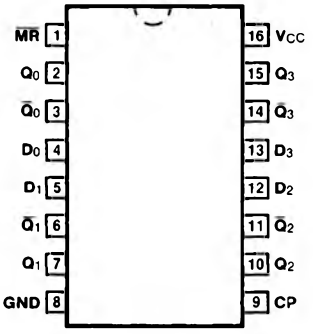
54/74175
54S/74S175
54LS/74LS175
QUAD D FLIP-FLOP

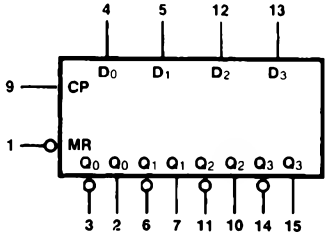
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '175 is a high speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **ASYNCHRONOUS COMMON RESET**
- **TRUE AND COMPLEMENT OUTPUT**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5% TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74175PC, 74S175PC 74LS175PC		9B
Ceramic DIP (D)	A	74175DC, 74S175DC 74LS175DC	54175DM, 54S175DM 54LS175DM	6B
Flatpak (F)	A	74175FC, 74S175FC 74LS175FC	54175FM, 54S175FM 54LS175FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$D_0 - D_3$	Data Inputs	1.0/1.0	1.25/1.25	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	1.25/1.25	0.5/0.25
$\overline{MR}$	Master Reset Input (Active LOW)	1.0/1.0	1.25/1.25	0.5/0.25
$Q_0 - Q_3$	True Outputs	20/10	25/12.5	10/5.0 (2.5)
$\overline{Q}_0 - \overline{Q}_3$	Complement Outputs	20/10	25/12.5	10/5.0 (2.5)

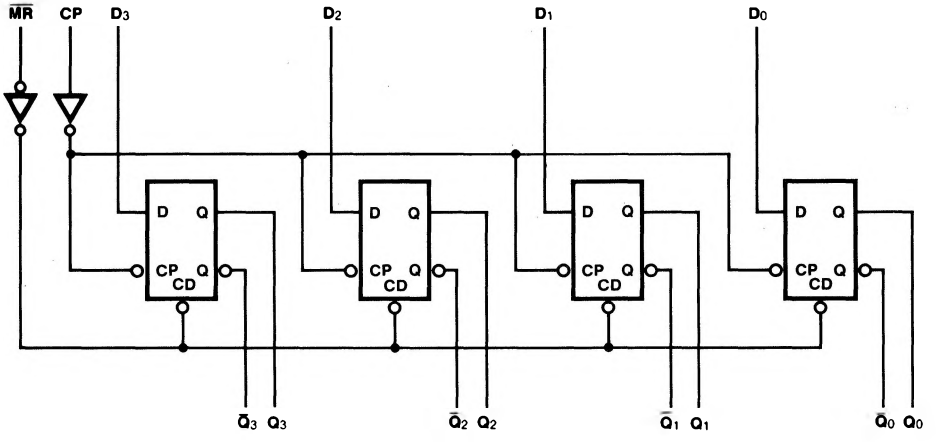
FUNCTIONAL DESCRIPTION — The '175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The '175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

INPUTS	OUTPUTS	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

t_n = Bit time before clock positive-going transition
t_{n+1} = Bit time after clock positive-going transition
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{CC}	Power Supply Current		45		96		18	mA	V_{CC} = Max D_n = $\overline{MR}$ = 4.5 V CP = ⎍

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		C_L = 15 pF R_L = 400 Ω		C_L = 15 pF R_L = 280 Ω		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	25		75		30		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		30 35		12 17		25 25	ns	Figs. 3-1, 3-8
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		35		22		33	ns	Figs. 3-1, 3-16
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$		25		15		24	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20		5.0 5.0		10 10		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0		3.0 3.0		5.0 5.0		ns	
t_w (H)	CP Pulse Width HIGH	20		7.0		15		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		7.0		18		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	25		5.0		12		ns	Fig. 3-16