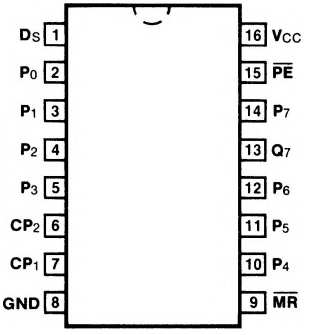
54/74166

8-BIT SHIFT REGISTER

DESCRIPTION — The '166 is an 8-bit, serial- or parallel-in, serial-out shift register using edge triggered D-type flip-flops. Serial and parallel entry are synchronous, with state changes initiated by the rising edge of the clock. An asynchronous Master Reset overrides other inputs and clears all flip-flops. The circuit can be clocked from two sources or one CP input can be used to trigger the other.

- **35 MHz TYPICAL SHIFT FREQUENCY**
- **ASYNCHRONOUS MASTER RESET**
- **SYNCHRONOUS PARALLEL ENTRY**
- **GATED CLOCK INPUT CIRCUITRY**

CONNECTION DIAGRAM
PINOUT A



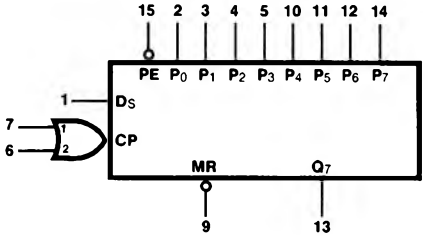
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74166PC		9B
Ceramic DIP (D)	A	74166DC	54166DM	7B
Flatpak (F)	A	74166FC	54166FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0
D_S	Serial Data Input	1.0/1.0
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0
P_0 — P_7	Parallel Data Inputs	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
Q_7	Last Stage Output	20/10

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

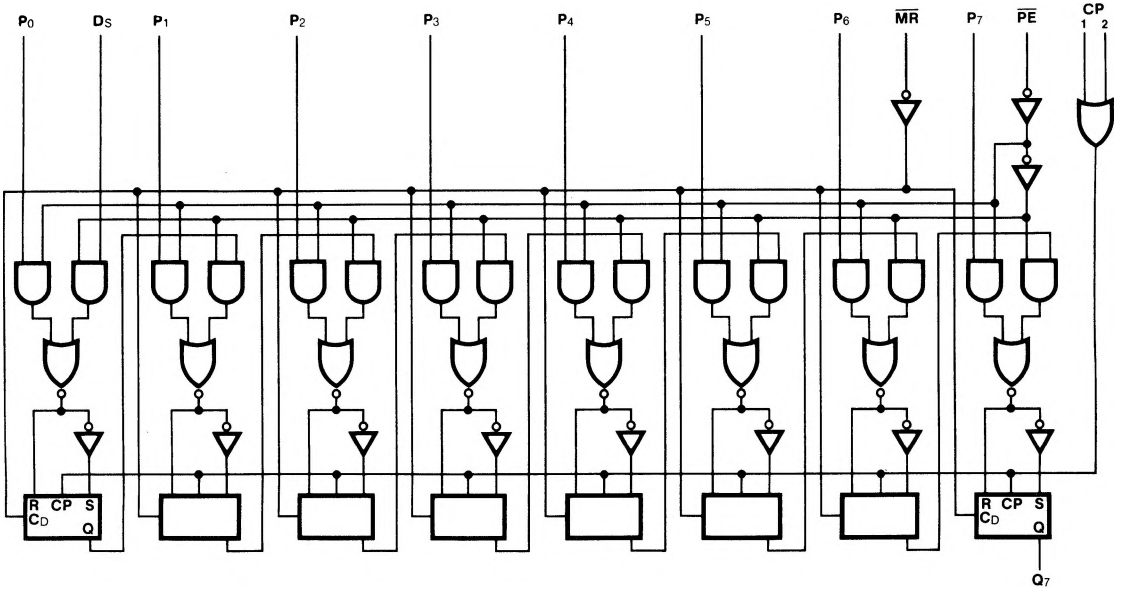
FUNCTIONAL DESCRIPTION — Operation is synchronous (except for Master Reset) and state changes are initiated by the rising edge of either clock input if the other clock input is LOW. When one of the clock inputs is used as an active HIGH clock inhibit, it should attain the HIGH state while the other clock is still in the HIGH state following the previous operation. When the Parallel Enable ($\overline{PE}$) input is LOW, data is loaded into the register from the Parallel Data ($P_0 - P_7$) inputs on the next rising edge of the clock. When $\overline{PE}$ is HIGH, information is shifted from the Serial Data (D_S) input to Q_0 and all data in the register is shifted one bit position (i.e., $Q_0 \rightarrow Q_1$, $Q_1 \rightarrow Q_2$, etc.) on the rising edge of the clock.

MODE SELECT TABLE

INPUTS				RESPONSE
$\overline{MR}$	$\overline{PE}$	CP_1	CP_2	
L	X	X	X	Asynchronous Reset; Q_n = LOW
H H	X X	H* X	X H*	Hold
H H	L L	L ↑	↑ L	Parallel Load; $P_n \rightarrow Q_n$
H H	H H	L ↑	↑ L	Shift; $D_S \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.

*The HIGH signal on one CP input must be established while the other CP input is HIGH.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		127	mA	V_{CC} = Max, CP_1 = ⎍⎍ D_S = 4.5 V CP_2, $\overline{MR}$, $\overline{PE}$, P_n = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF R_L = 400 Ω		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	25		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_7		26 30	ns	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_7		35	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S or P_n to CP_n	20 20		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S or P_n to CP_n	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP_n	30 30		ns	
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP_n	0 0		ns	
t_w (H)	CP_n Pulse Width HIGH	20		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16