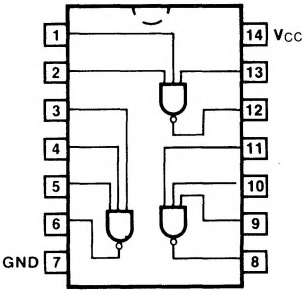
54/7412

TRIPLE 3-INPUT NAND GATE

(With Open-Collector Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7412PC		9A
Ceramic DIP (D)	A	7412DC	5412DM	6A
Flatpak (F)	A	7412FC	5412FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Inputs	1.0/1.0
Outputs	OC**/10

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		6.0	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}			16.5		V_{IN} = Open	
t_{PLH}	Propagation Delay		45	ns	Figs. 3-2, 3-4	
t_{PHL}			15			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.

**OC — Open Collector