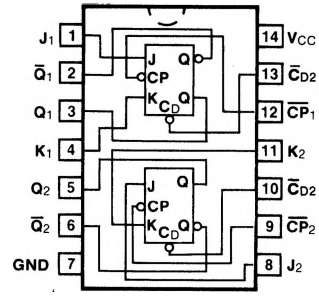
54/74107
54LS/74LS107

DUAL JK FLIP-FLOP
(With Separate Clears and Clocks)

DESCRIPTION — The '107 dual JK master/slave flip-flops have a separate clock for each flip-flop. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) isolate slave from master; 2) enter information from J and K inputs to master; 3) disable J and K inputs; 4) transfer information from master to slave.

CONNECTION DIAGRAM
PINOUT A



TRUTH TABLE

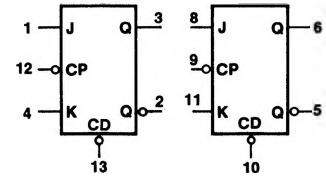
INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM

Asynchronous Input:
LOW input to $\bar{C}_D$ sets Q to LOW level
Clear is independent of clock

LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

The 'LS107 offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock is HIGH and the bistable will perform according to the Truth Table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

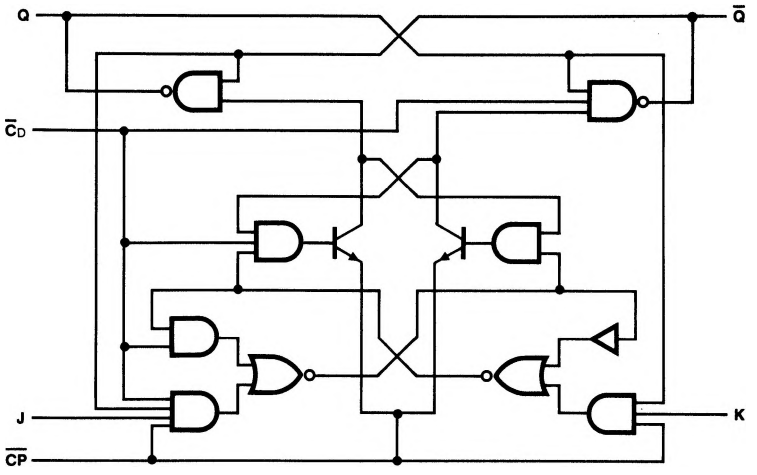
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +125°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74107PC, 74LS107PC		9A
Ceramic DIP (D)	A	74107DC, 74LS107DC	54107DM, 54LS107DM	6A
Flatpak (F)	A	74107FC, 74LS107FC	54107FM, 54LS107FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
J_1, J_2, K_1, K_2	Data Inputs	1.0/1.0	0.5/0.25
$\overline{CP}_1$, $\overline{CP}_2$	Clock Pulse Inputs (Active Falling Edge)	2.0/2.0	2.0/0.5
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0	1.5/0.5
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	20/10	10/5.0 (2.5)

LOGIC DIAGRAM (one half shown)



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current		40		8.0	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω Min	54/74 Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
f_{max}	Maximum Clock Frequency	15		30		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}_n$ to Q_n or $\overline{Q}_n$		25 40		20 30	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ to Q_n or $\overline{Q}_n$		25 40		20 30	ns	Figs. 3-1, 3-10

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_s (H)	Setup Time HIGH J_n or K_n to $\overline{CP}_n$	0		20		ns	Fig. 3-18 ('107) Fig. 3-7 ('LS107)
t_h (H)	Hold Time HIGH J_n or K_n to $\overline{CP}_n$	0		0		ns	
t_s (L)	Setup Time LOW J_n or K_n to $\overline{CP}_n$	0		20		ns	
t_h (L)	Hold Time LOW J_n or K_n to $\overline{CP}_n$	0		0		ns	
t_w (H) t_w (L)	$\overline{CP}_n$ Pulse Width	20 47		13.5 20		ns	Fig. 3-9
t_w (L)	$\overline{C}_{Dn}$ Pulse Width LOW	25		25		ns	Fig. 3-10