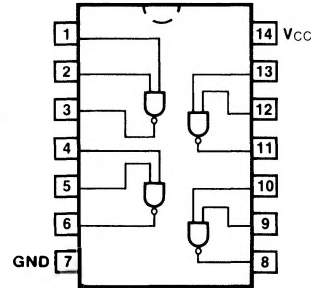


54/7403
54S/74S03
54LS/74LS03

QUAD 2-INPUT NAND GATE
 (With Open-Collector Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{ C to } +70^\circ\text{ C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{ C to } +125^\circ\text{ C}$	
Plastic DIP (P)	A	7403PC, 74S03PC 74LS03PC		9A
Ceramic DIP (D)	A	7403DC, 74S03DC 74LS03DC	5403DM, 54S03DM 54LS03DM	6A
Flatpak (F)	A	7403FC, 74S03FC 74LS03FC	5403FM, 54S03FM 54LS03FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	OC**/10	OC**/12.5	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74		54/74S		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max	Min	Max		$V_{IN} = \text{Gnd}$	$V_{CC} = \text{Max}$
I_{CCH}	Power Supply Current	8.0		13.2		1.6		mA		
I_{CCL}		22		36		4.4			$V_{IN} = \text{Open}$	
t_{PLH} t_{PHL}	Propagation Delay	45		2.0	7.5	22		mA	Figs. 3-2, 3-4	
		15		2.0	7.0	18				

*DC limits apply over operating temperature range; AC limits apply at $T_A = +25^\circ\text{ C}$ and $V_{CC} = +5.0\text{ V}$.

**OC — Open Collector