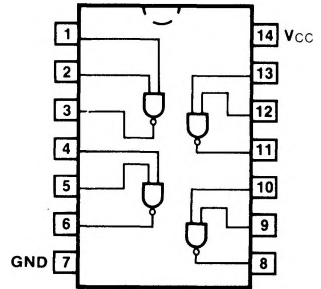


54/7400
54H/74H00
54S/74S00
54LS/74LS00
 QUAD 2-INPUT NAND GATE

CONNECTION DIAGRAMS
PINOUT A



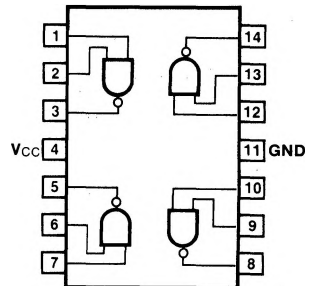
ORDERING CODE: See Section 9

| PKGS | PIN OUT | COMMERCIAL GRADE | MILITARY GRADE | PKG TYPE |
|-----------------|---------|---|---|----------|
| | | $V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{ C to } +70^\circ\text{ C}$ | $V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{ C to } +125^\circ\text{ C}$ | |
| Plastic DIP (P) | A | 7400PC, 74H00PC 74LS00PC, 74S00PC | | 9A |
| Ceramic DIP (D) | A | 7400DC, 74H00DC 74LS00DC, 74S00DC | 5400DM, 54H00DM 54LS00DM, 54S00DM | 6A |
| Flatpak (F) | A | 74LS00FC, 74S00FC | 54LS00FM, 54S00FM | 3I |
| | B | 7400FC, 74H00FC | 5400FM, 54H00FM | |

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

| PINS | 54/74 (U.L.) HIGH/LOW | 54/74H (U.L.) HIGH/LOW | 54/74S (U.L.) HIGH/LOW | 54/74LS (U.L.) HIGH/LOW |
|---------|-----------------------|------------------------|------------------------|-------------------------|
| Inputs | 1.0/1.0 | 1.25/1.25 | 1.25/1.25 | 0.5/0.25 |
| Outputs | 20/10 | 12.5/12.5 | 25/12.5 | 10/5.0 (2.5) |

PINOUT B



DC AND AC CHARACTERISTICS: See Section 3*

| SYMBOL | PARAMETER | 54/74 | | 54/74H | | 54/74S | | 54/74LS | | UNITS | CONDITIONS | |
|-----------|-------------------|-------|------|--------|-----|--------|-----|---------|----------------|-------|---|-----------------------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | $V_{IN} = \text{Gnd}$ $V_{IN} = \text{Open}$ | $V_{CC} = \text{Max}$ |
| I_{CCH} | Power Supply | 8.0 | 16.8 | 16 | 1.6 | mA | | | | | | |
| I_{CCL} | Current | 22 | 40 | 36 | 4.4 | | | | | | | |
| t_{PLH} | Propagation Delay | 22 | 10 | 2.0 | 4.5 | ns | | | Figs. 3-1, 3-4 | | | |
| t_{PHL} | | 15 | 10 | 2.0 | 5.0 | | | | | | 10 | |

*DC limits apply over operating temperature range; AC limits apply at $T_A = +25^\circ\text{ C}$ and $V_{CC} = +5.0\text{ V}$.