

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The 515 is a general purpose high-gain amplifier with differential input and output. It is fabricated within a monolithic silicon substrate by planar and epitaxial techniques. A pair of compensation points is provided to allow frequency compensation for stable closed loop operation.

This device is not internally referenced to ground and with proper input bias may be operated from a single power supply.

FEATURES

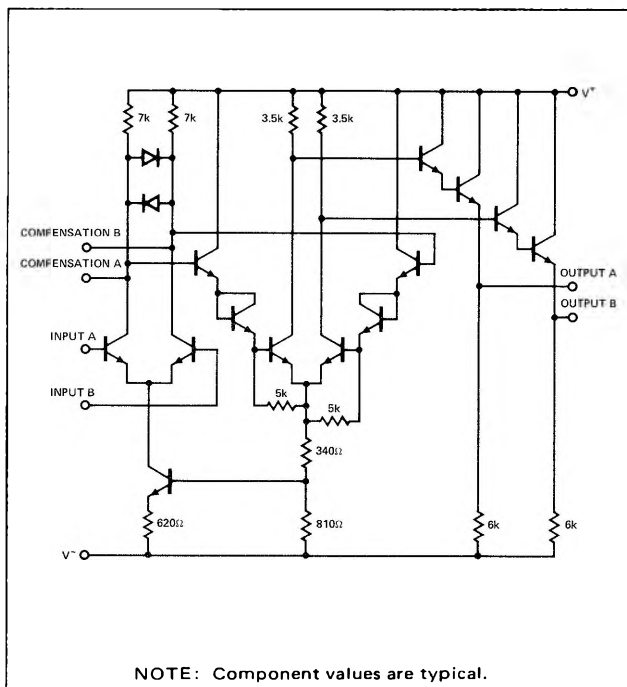
- DIFFERENTIAL VOLTAGE GAIN (Open Loop) = 4,500
- INPUT OFFSET VOLTAGE = 0.5mV
- INPUT OFFSET VOLTAGE STABILITY = $5.0\mu\text{V}/^\circ\text{C}$
- INPUT COMMON MODE RANGE = +1.5V, -1.0V
- COMMON MODE REJECTION RATIO = 100dB
- BANDWIDTH (Open Loop) = 1.0 MHz

ABSOLUTE MAXIMUM RATINGS

Applied Voltage (V^+ to V^-)	12V
Differential Input Voltage (V_5 to V_7)	$\pm 5.0\text{V}$
Input Current (I_5, I_7)	$\pm 2.0\text{mA}$
Output Current (I_2, I_{10})	$\pm 30\text{mA}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Operating Temperature	0°C to $+75^\circ\text{C}$
Junction Temperature	150°C

Maximum ratings are limiting values above which serviceability may be impaired.

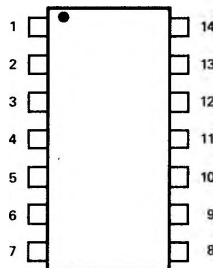
EQUIVALENT CIRCUIT



PIN CONFIGURATIONS

A PACKAGE

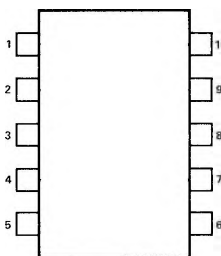
(Top View)



1. Input B
2. NC
3. NC
4. Compensation
5. NC
6. Output B
7. V^-
8. Output A
9. NC
10. NC
11. Compensation
12. NC
13. Input A
14. V^+

ORDER PART NO. NE515A

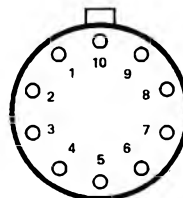
G PACKAGE



1. V^-
2. Output A
3. NC
4. Compensation
5. Input A
6. V^+
7. Input B
8. Compensation
9. NC
10. Output B

ORDER PART NOS. SE515G/NE515G

K PACKAGE



1. V^-
2. Output A
3. NC
4. Compensation
5. Input A
6. V^+
7. Input B
8. Compensation
9. NC
10. Output B

ORDER PART NOS. SE515K/NE515K

SIGNETICS ■ 515 – DIFFERENTIAL AMPLIFIER

SE515 ELECTRICAL CHARACTERISTICS (Standard Conditions: $V_7 = 0V$, $V_1 = -3.0V$; Notes: 4, 5, 6, 7, 8, 9)

CHARACTERISTIC	$V_6 = +4.0V$	$V_6 = +6.0V$			UNITS	TEMP	TEST CONDITIONS
	TYP	MIN	TYP	MAX			
Open Loop Voltage Gain (dc)	2,500	3,500	4,500		V/V	+25°C	Note 2
	1,800		3,000		V/V	+125°C	
Open Loop Voltage Gain (ac)	2,000	2,500	3,500		V/V	+25°C	f = 800 kHz
Input Offset Voltage	0.5		0.5	3.0	mV	-55°C	Note 1
	0.5		0.5	2.0	mV	+25°C	
	0.5		0.5	3.0	mV	+125°C	
Input Bias Current	18		25	40	μA	-55°C	Note 1
	12		16	24	μA		
Differential Input Resistance	2.0	1.0	1.5		k Ω	-55°C	Note 10
	4.0	2.0	3.2		k Ω	+25°C	
Input Common Mode Range	± 1.0		+1.5		V	+25°C	
			-1.0				
Balanced Output dc Level	-0.1		+1.2	+1.8	V	-55°C	Note 1
	+0.3		+1.6		V	+25°C	
	+0.6		+1.9		V	+125°C	
Output Voltage Swing	4.7	5.7	6.3		V	-55°C	Note 3
	4.7	5.7	6.3		V	+25°C	
	4.7	5.7	6.3		V	+125°C	
High Output Level	+2.3	+4.0	+4.3		V	-55°C	$V_5 = 10mV$
	+2.6	+4.3	+4.6		V	+25°C	
	+3.0	+4.7	+5.0		V	+125°C	
Low Output Level	-2.4	-1.7	-2.0		V	-55°C	$V_5 = 10mV$
	-2.1	-1.4	-1.7		V	+25°C	
	-1.7	-1.0	-1.3		V	+125°C	
Output Resistance	100		100		Ω	+25°C	Note 1
Common Mode Rejection Ratio	100		100		dB		
Power Supply Current	3.5		5.5	7.0		mA	Note 1
				7.0		mA	
				7.0		mA	

NOTES:

- Adjust V_5 to obtain $V_2 = V_{10}$.
- Output voltage swing = 1.3V peak to peak.
- Output voltage swing is guaranteed by output voltage limit tests.
- Voltage and current subscripts refer to pin numbers.
- All measurements are referenced to power supply common. Positive current flow is defined as into the terminal indicated.
- All specifications herein apply for interchange of voltages and currents at Pins 5 and 7.
- Acceptance Test Sub-Group references apply to minimum and maximum limits only.
- The SE515K has Pins 1, 3 and 9 connected to the case. The SE515G has Pins 3 and 9 open.
- See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance Test Sub-Groups. Sub-Group A-7 is used for electrical end points for Linear Products.
- Differential Input Resistance is computed from input bias current.

NE515 ELECTRICAL CHARACTERISTICS (Standard Conditions: $V_B = 0V$, $V_A = 3.0V$; Notes: 4, 5, 6, 7, 8, 9)

CHARACTERISTIC	$V_F = +4.0V$	$V_F = +6.0V$			UNITS	TEMP	TEST CONDITIONS
	TYP	MIN	TYP	MAX			
Open Loop Voltage Gain (dc)	1,800	2,500	3,200		V/V	+25°C	Note 2
	1,350		2,200		V/V	+75°C	
Open Loop Voltage Gain (ac)	1,500	1,700	2,500		V/V	+25°C	f = 800 kHz
Input Offset Voltage	0.5		0.5	4.0	mV	0°C	Note 1
	0.5		0.5	3.0	mV	+25°C	
	0.5		0.5	4.0	mV	+75°C	
Input Bias Current	18		25	40	μA	0°C	Note 1
	15		20	31	μA	+25°C	
Differential Input Resistance	3.2	1.4	2.3		k Ω	0°C	Note 10
	3.5	1.7	2.6		k Ω	+25°C	
Input Common Mode Range	± 1.0		+1.5		V	+25°C	
			-1.0				
Balanced Output dc Level	-0.1		+1.2	+1.8	V	0°C	Note 1
	+0.3		+1.6		V	+25°C	
	+0.6		+1.9		V	+75°C	
Output Voltage Swing	4.5	5.3	6.1		V	0°C	Note 3
	4.5	5.3	6.1		V	+25°C	
	4.5	5.3	6.1		V	+75°C	
High Output Level	+2.3	+3.9	+4.3		V	0°C	$V_C = 10mV$
	+2.5	+4.1	+4.5		V	+25°C	
	+2.8	+4.3	+4.8		V	+75°C	
Low Output Level	-2.2	-1.4	-1.8		V	0°C	$V_C = 10mV$
	-2.0	-1.2	-1.6		V	+25°C	
	-1.7	-1.0	-1.3		V	+75°C	
Output Resistance	100		100		Ω	+25°C	Note 1
Common Mode Rejection Ratio	100		100		dB	+25°C	
Power Supply Current	3.5		5.5	7.0	mA	0°C	Note 1
				7.0	mA	+25°C	
				7.0	mA	+75°C	

Letter subscripts refer to pins on circuit schematic.

NOTES:

- Adjust V_C to obtain $V_G = V_H$.
- Output voltage swing = 1.3V peak to peak.
- Output voltage swing is guaranteed by output voltage limit tests.
- Voltage and current subscripts refer to pin numbers.
- All measurements are referenced by power supply common. Positive current flow is defined as into the terminal indicated.
- All specifications herein apply for interchange of voltages and currents at Pins B and C.
- Acceptance Test Sub-Group references apply to minimum and maximum limits only.
- The NE515K has Pins 1, 3 and 9 connected to the case. The NE515G has Pins 3 and 9 open.
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- Differential Input Resistance is computed from input bias current.