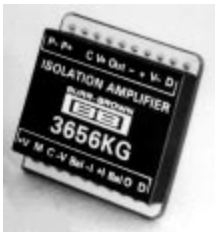
BURR - BROWN®



3656

Transformer Coupled ISOLATION AMPLIFIER

FEATURES

- INTERNAL ISOLATED POWER
- 8000V ISOLATION TEST VOLTAGE
- 0.5μA MAX LEAKAGE AT 120V, 60Hz
- 3-PORT ISOLATION
- IMR: 125dB REJECTION AT 60Hz
- 1" x 1" x 0.25" CERAMIC PACKAGE

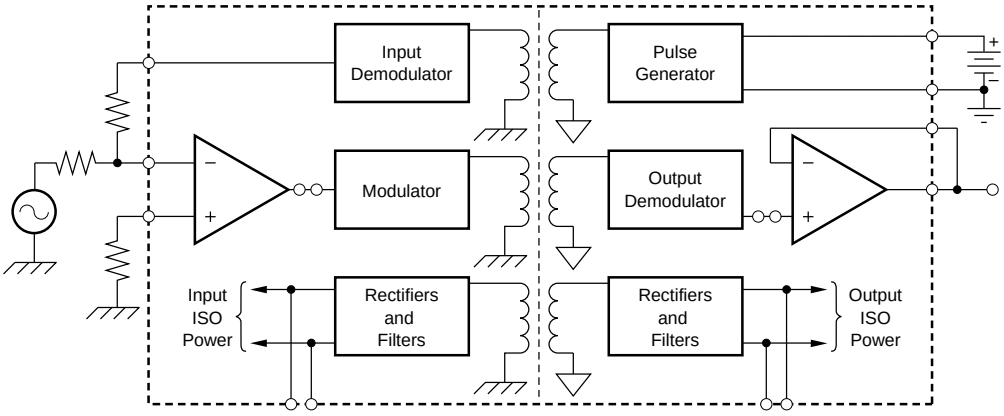
APPLICATIONS

- MEDICAL
  Patient Monitoring and Diagnostic Instrumentation
- INDUSTRIAL
  Ground Loop Elimination and Off-ground Signal Measurement
- NUCLEAR
  Input/Output/Power Isolation

DESCRIPTION

The 3656 was the first amplifier to provide a total isolation function, both signal and power isolation, in integrated circuit form. This remarkable advancement in analog signal processing capability was accomplished by use of a patented modulation technique and miniature hybrid transformer.

Versatility and performance are outstanding features of the 3656. It is capable of operating with three completely independent grounds (three-port isolation). In addition, the isolated power generated is available to power external circuitry at either the input or output. The uncommitted op amps at the input and the output allow a wide variety of closed-loop configurations to match the requirements of many different types of isolation applications.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

At +25°C, V± = 15VDC and 15VDC between P+ and P–, unless otherwise specified.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG MIN	TYP	MAX	UNITS
ISOLATION					
Voltage					
Rated Continuous[1], DC		3500 (1000)			VDC
Test, 10s[1]		8000 (3000)			VDC
Test, 60s[1]	G_1 = 10V/V	2000 (700)			Vrms
Rejection					
DC			160		dB
60Hz, < 100Ω in I/P Com[2]			125		dB
60Hz, 5kΩ in I/P Com[2]					
3656HG		108			dB
3656AG, BG, JG, KG		112			dB
Capacitance[1]			6 (6.3)		pF
Resistance[1]			10^{12} (10^{12})		Ω
Leakage Current	120V, 60Hz		0.28	0.5	µA
GAIN					
Equations	See Text				
Accuracy of Equations					
Initial[3] 3656HG	G < 100V/V			1.5	%
3656AG, JG, KG				1	%
3656BG				0.3	%
vs Temperature 3656HG				480	ppm/°C
3656AG, JG				120	ppm/°C
3656BG, KG				60	ppm/°C
vs Time			0.02 (1 + log khrs.)		%
Nonlinearity	$R_A + R_F = R_B \geq 2M\Omega$				
External Supplies Used at					
Pins 12 and 16, 3656HG	Unipolar or Bipolar Output			±0.15	%
3656AG, JG, KG				±0.1	%
3656BG				±0.05	%
Internal Supplies Used for	Bipolar Output Voltage				
Output Stage	Swing, Full Load[4]		±0.15		%
OFFSET VOLTAGE[5], RTI					
Initial[3], 3656HG	15Vp between P+ and P–			±[4 + (40/G_1)]	mV
3656AG, JG				±[2 + (20/G_1)]	mV
3656BG, KG				±[1 + (10/G_1)]	mV
vs Temperature, 3656HG				±[200 + (1000/G_1)]	µV/°C
3656JG				±[50 + (750/G_1)]	µV/°C
3656AG				±[25 + (500/G_1)]	µV/°C
3656KG				±[10 + (350/G_1)]	µV/°C
3656BG				±[5 + (350/G_1)]	µV/°C
vs Supply Voltage	Supply between P+ and P–				
3656HG				±[0.6 + (3.5/G_1)]	mV/V
3656AG, BG, JG, KG				±[0.3 + (2.1/G_1)]	mV/V
vs Current[6]			±[0.1 + (10/G_1)]	±[0.2 + (20/G_1)]	mV/mA
vs Time			±[10 + (100/G_1)] • (1 + log khrs.)		µV
AMPLIFIER PARAMETERS, Apply to A_1 and A_2					
Bias Current[7]					
Initial				100	nA
vs Temperature			0.5		nA/°C
vs Supply			0.2		nA/V
Offset Current[7]			5	20	nA
Impedance	Common-Mode		100 || 5		MΩ || pF
Input Noise Voltage	f_B = 0.05Hz to 100Hz		5		µVp-p
	f_B = 10Hz to 10kHz		5		µVrms
Input Voltage Range[8]					
Linear Operation	Internal Supply			±5	V
	External Supply			Supply –5	V
Output Current	V_{OUT} = ±5V				
	±15V External Supply	±5			mA
	Internal Supply	±2.5			mA
	V_{OUT} = ±10V				
	±15V External Supply	±2.5			mA
	V_{OUT} = ±2V, $V_{P+, P-}$ = 8.5V				
	Internal Supply		±1		mA
Quiescent Current			150	450	µA

SPECIFICATIONS (CONT)

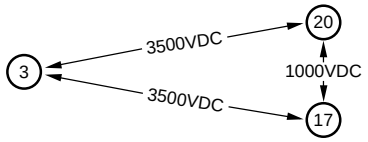
ELECTRICAL

At +25°C, V± = 15VDC and 15VDC between P+ and P–, unless otherwise specified.

PARAMETER	CONDITIONS	3656AG, BG, HG, JG, KG MIN	TYP	MAX	UNITS
FREQUENCY RESPONSE					
±3dB Response	Small Signal		30		kHz
Full Power			1.3		kHz
Slew Rate	Direction Measured at Output	+0.1, –0.04			V/µs
Settling Time	to 0.05%		500		µs
OUTPUT					
Noise Voltage (RTI)	f_B = 0.05Hz to 100Hz		$\sqrt{(5)^2 + (22/G_1)^2}$		µVp-p
	f_B = 10Hz to 10kHz		$\sqrt{(5)^2 + (11/G_1)^2}$		µVrms
Residual Ripple[9]			5		mVp-p
POWER SUPPLY IN, at P+, P–					
Rated Performance			15		VDC
Voltage Range[10]	Derated Performance	8.5		16	VDC
Ripple Current[9]			10	25	mAp-p
Quiescent Current[11]	Average		14	18	mA/DC
Current vs Load Current[12]	vs Current from +V, –V, V+, V–		0.7		mA/mA
ISOLATED POWER OUT, At +V, –V, V+, V– pins[13]					
Voltage, No Load	15V Between P+ and P–	8.5	9	9.5	V
Voltage, Full Load	±5mA (10mA sum) Load[12]	7	8	9	V
Voltage vs Power Supply	vs Supply Between P+ and P–		0.66		V/V
Ripple Voltage[9]					
No Load			40		mVp-p
Full Load	±5mA Load		80	200	mVp-p
TEMPERATURE RANGE					
Specification 3656AG, BG		–25		+85	°C
3656HG, JG, KG		0		+70	°C
Operation[10]		–55		+100	°C
Storage[14]		–65		+125	°C

NOTES: (1) Ratings in parenthesis are between P- (pin 20) and O/P Com (pin 17). Other isolation ratings are between I/P Com and O/P Com or I/P Com and P–. (2) See Performance Curves. (3) May be trimmed to zero. (4) If output swing is unipolar, or if the output is not loaded, specification same as if external supply were used. (5) Includes effects of A_1 and A_2 offset voltages and bias currents if recommended resistors used. (6) Versus the sum of all external currents drawn from V+, V–, +V, –V (= ISO). (7) Effects of A_1 and A_2 bias currents and offset currents are included in Offset Voltage specifications. (8) With respect to I/P Com (pin 3) for A_1 and with respect to O/P Com (pin 17) for A_2. CMR for A_1 and A_2 is 100dB, typical. (9) In configuration of Figure 3. Ripple frequency approximately 750kHz. Measurement bandwidth is 30kHz. (10) Decreases linearly from 16VDC at 85°C to 12VDC at 100°C. (11) Instantaneous peak current required from pins 19 and 20 at turn-on is 100mA for slow rising voltages (50ms) and 300mA for fast rises (50µs). (12) Load current is sum drawn form +V, –V, V+, V– (= I_{ISO}). (13) Maximum voltage rating at pins 1 and 4 is ±18VDC; maximum voltage rating at pins 12 and 16 is ±18VDC. (14) Isolation ratings may degrade if exposed to 125°C for more than 1000 hours or 90°C for more than 50,000 hours.

Example of the ratings for 3-port continuous isolation.



PIN DESIGNATIONS

NO.	DESCRIPTION	NO.	DESCRIPTION
1	+V	11	Output DEMOD
2	MOD Input	12	V–
3	Input DEMOD COM	13	A_2 Noninverting Input
4	–V	14	A_2 Inverting Input
5	Balance	15	A_2 Output
6	A_1 Inverting Input	16	V+
7	A_1 Noninverting Input	17	Output DEMOD COM
8	Balance	18	No Pin
9	A_1 Output	19	P+
10	Input DEMOD	20	P–

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
3656	20-Lead ISO Omni	102A

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

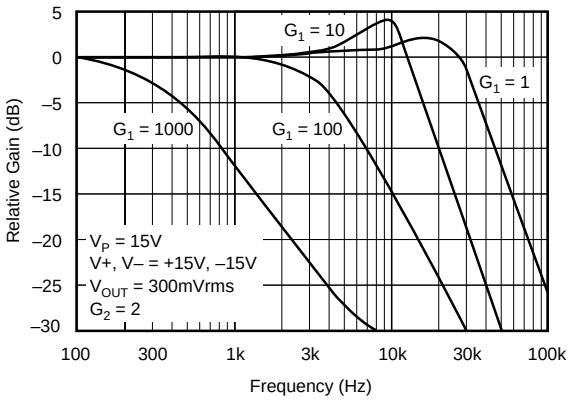
Supply Without Damage 16V
Input Voltage Range Using Internal Supply ..... ±8V
Input Voltage Range Using External Supply ..... Supply
Continuous Isolation Voltage[1] ..... 3500, (1000) VDC
Storage Temperature ..... –65°C to +125°C
Lead Temperature, (soldering, 10s) ..... +300°C

NOTE: (1) Ratings in parenthesis are between P– (pin 20) and O/P Com (pin 17). Other isolation ratings are between I/P Com and O/P Com or I/P Com and P–.

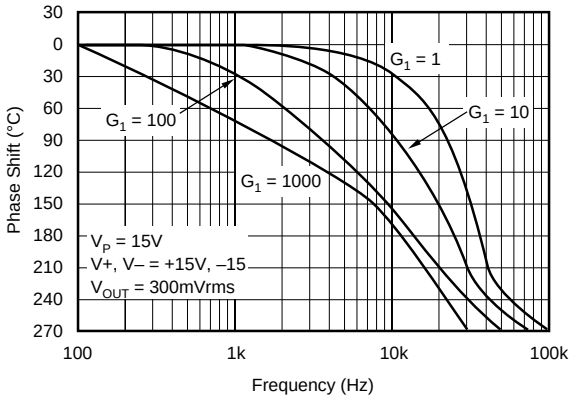
TYPICAL PERFORMANCE CURVES

All specifications typical at +25°C, unless otherwise specified.

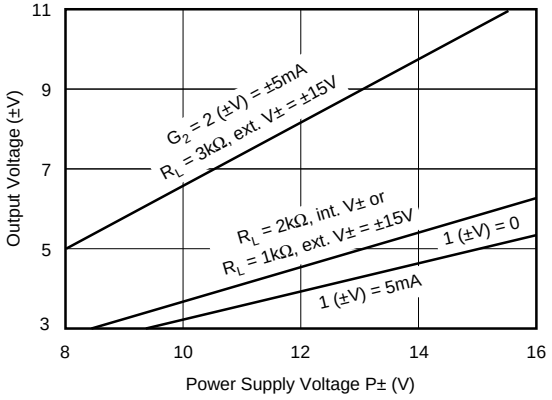
SMALL SIGNAL FREQUENCY RESPONSE



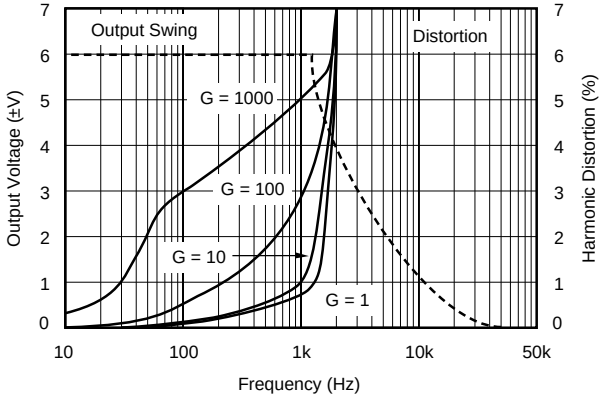
PHASE RESPONSE



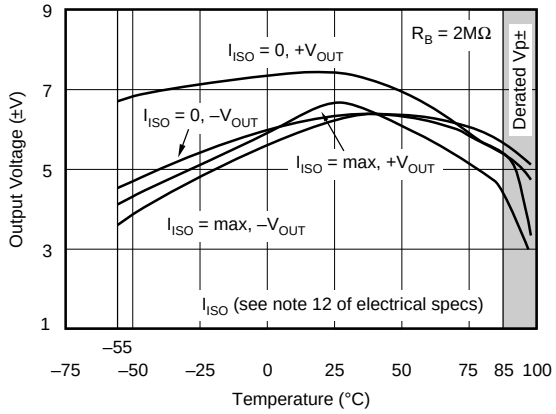
OUTPUT SWING vs SUPPLY VOLTAGE



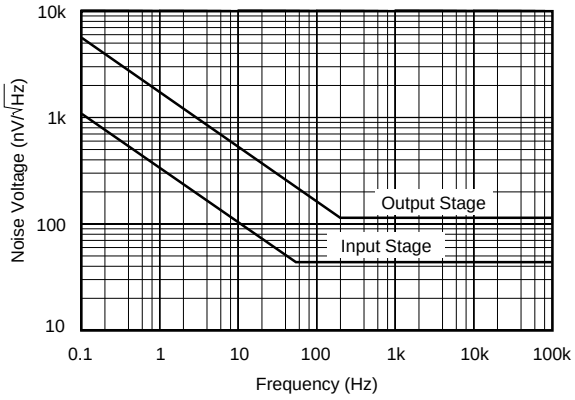
OUTPUT SWING AND DISTORTION vs FREQUENCY



OUTPUT VOLTAGE SWING vs TEMPERATURE
AND ISOLATED SUPPLY LOAD



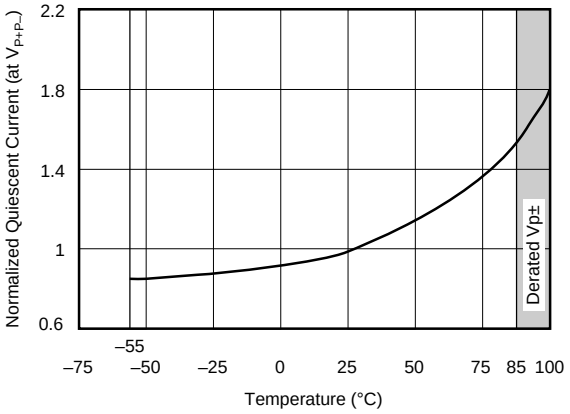
NOISE VOLTAGE vs FREQUENCY



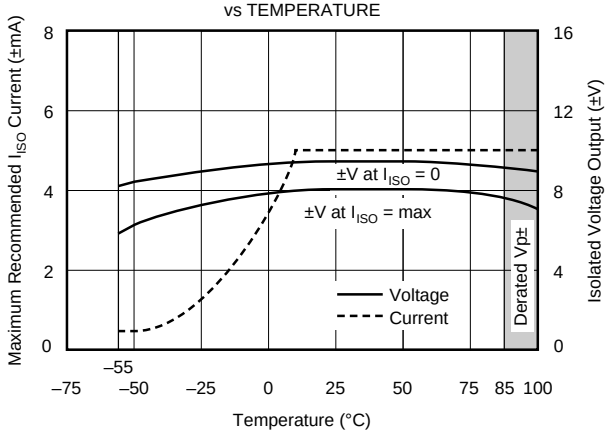
TYPICAL PERFORMANCE CURVES (CONT)

All specifications typical at +25°C, unless otherwise specified.

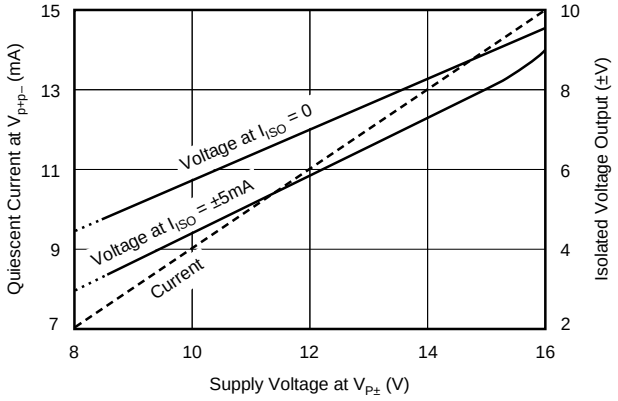
QUIESCENT CURRENT vs TEMPERATURE



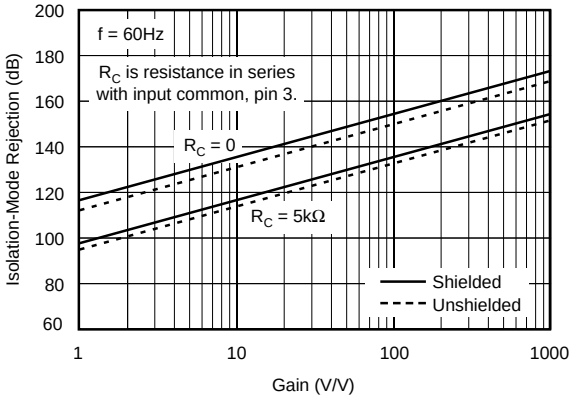
ISOLATED OUTPUT VOLTAGE AND CURRENT vs TEMPERATURE



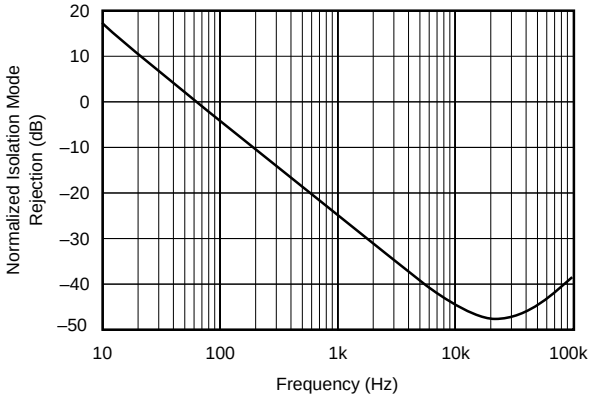
QUIESCENT CURRENT AND ISOLATED VOLTAGE OUTPUT vs SUPPLY VOLTAGE



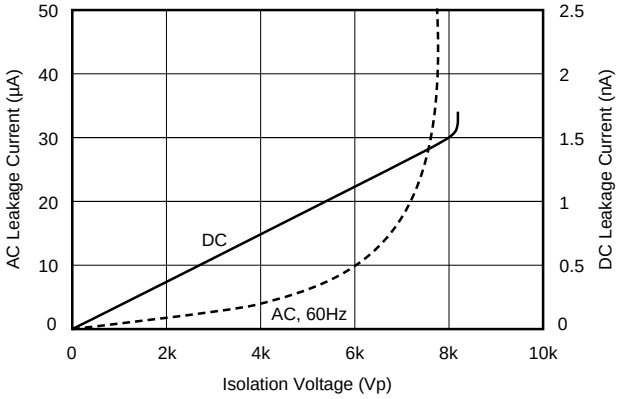
ISOLATION-MODE REJECTION vs GAIN



ISOLATION MODE REJECTION vs FREQUENCY



AC AND DC LEAKAGE CURRENT vs ISOLATION VOLTAGE



THEORY OF OPERATION

Details of the 3656 are shown in Figure 1. The external connections shown, place it in its simplest gain configuration —unity gain, noninverting. Several other amplifier gain configurations and power isolation configurations are possible. See Installation and Operating Instructions and Applications sections for details.

Isolation of both signal and power is accomplished with a single miniature toroid transformer with multiple windings. A pulse generator operating at approximately 750kHz provides a two-part voltage waveform to transformer, T_1. One part of the waveform is rectified by diodes D_1 through D_4 to provide the isolated power to the input and output stages (+V, –V and V+, V–). The other part of the waveform is modulated with input signal information by the modulator operating into the V_2 winding of the transformer.

The modulated signal is coupled by windings W_6 and W_7 to two matched demodulators—one in the input stage and one in the output stage—which generate identical voltages at their outputs, pins 10 and 11 (Voltages identical with respect to their respective commons, pins 3 and 17). In the input stage the input amplifier, A_1, the modulator and the input demodulator are connected in a negative feedback loop. This forces the voltage at pin 6 (connect as shown in Figure 1) to equal the input signal voltage applied at pin 7. Since the input and the output demodulators are matched and produce identical output voltages, the voltage at pin 11 (referenced to pin 17, the output common) is equal to the voltage at pin 10 (referenced to pin 3, the input common). In the output stage, output amplifier A_2 is connected as a unity gain buffer, thus the output voltage at pin 15 equals the output demodulator voltage at pin 11. The end result is an isolated output voltage at pin 15 equal to the input voltage at pin 7 with no galvanic connection between them.

Several amplifier and power connection variations are possible:

1. The input stage may be connected in various operational amplifier gain configurations.
2. The output stage may be operated at gains above unity.
3. The internally generated isolated voltages which provide power to A_1 and A_2 may be overridden and external supply voltages used instead.

Versatility and its three independent isolated grounds allow simple solutions to demanding analog signal conditioning problems. See the Installation and Operating Instructions and Applications sections for details.

INSTALLATION AND OPERATING INSTRUCTIONS

The 3656 is a very versatile device capable of being used in a variety of isolation and amplification configurations. There are several fundamental considerations that determine configuration and component value constraints:

1. Consideration must be given to the load placed on the resistance (pin 10 and pin 11) by external circuitry. Their output resistance is 100kΩ and a load resistor of 2MΩ or greater is recommended to prevent a voltage divider loading effect in excess of 5%.

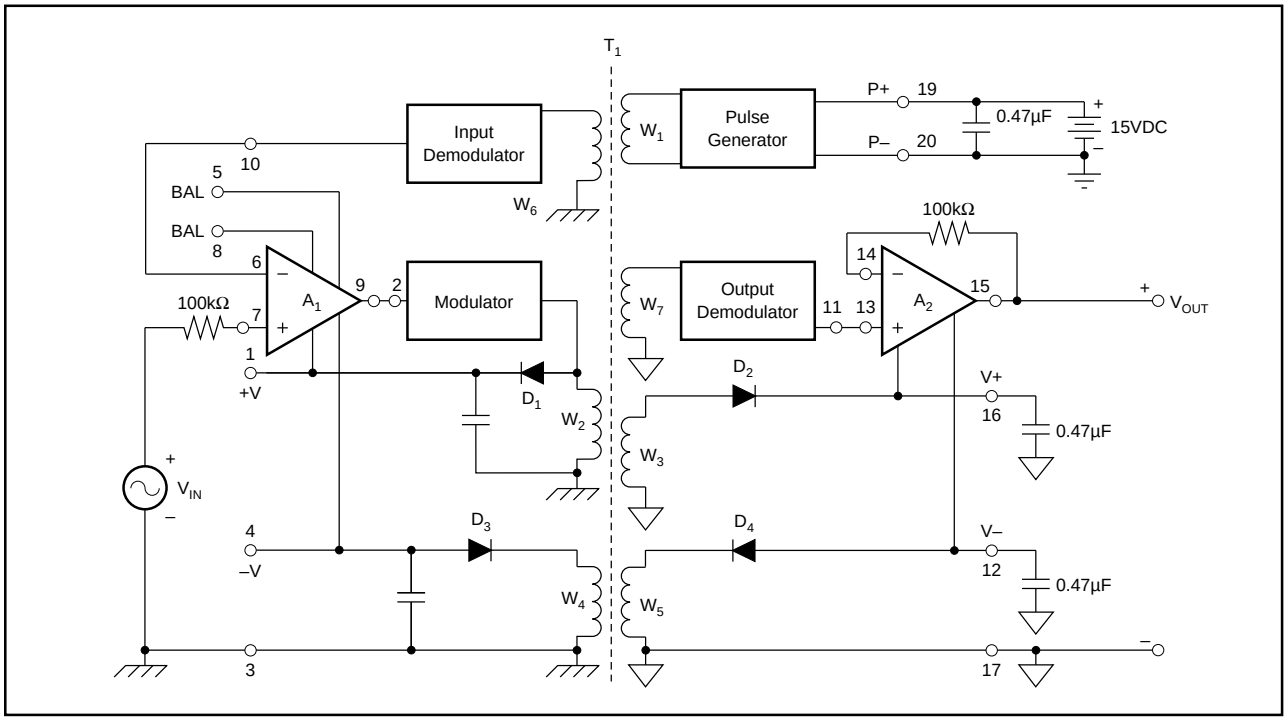


FIGURE 1. Block Diagram.

2. Demodulator loadings should be closely matched so their output voltages will be equal. (Unequal demodulator output voltages will produce a gain error.) At the 2MΩ level, a matching error of 5% will cause an additional gain error of 0.25%.
3. Voltage swings at demodulator outputs should be limited to 5V. The output may be distorted if this limit is exceeded. This constrains the maximum allowed gains of the input and output stages. Note that the voltage swings at demodulator outputs are tested with 2MΩ load for a minimum of 5V.
4. Total current drawn from the internal isolated supplies must be limited to less than ±5mA per supply and limited to a total of 10mA. In other words, the combination of external and internal current drawn from the internal circuitry which feeds the +V, –V, V+ and V– pins should be limited to 5mA per supply (total current to +V, –V, V+ and V– limited to 10mA). The internal filter capacitors for ±V are 0.01µF. If more than 0.1mA is drawn to provide isolated power for external circuitry (see Figure 12), additional capacitors are required to provide adequate filtering. A minimum of 0.1µF/mA is recommended.
5. The input voltage at pin 7 (noninverting input to A_1) must not exceed the voltage at pin 4 (negative supply voltage for A_1) in order to prevent a possible lockup condition. A low leakage diode connected between pins 7 and 4, as shown in Figure 2, can be used to limit this input voltage swing.
6. Impedances seen by each amplifier's + and – input terminals should be matched to minimize offset voltages caused by amplifier input bias currents. Since the demodulators have a 100kΩ output resistance, the amplifier input not connected to the demodulator should also see 100kΩ.
7. All external filter capacitors should be mounted as close to the respective supply pins as possible in order to prevent excessive ripple voltages on the supplies or at the output. (Optimum spacing is less than 0.5". Ceramic capacitors recommended.)

POWER AND SIGNAL CONFIGURATIONS

NOTE: Figures 2, 3 and 4 are used to illustrate both signal and power connection configurations. In the circuits shown, the power and signal configurations are independent so that any power configuration could be used with any signal configuration.

ISOLATED POWER CONFIGURATIONS

The 3656 is designed with isolation between the input, the output, and the power connections. The internally generated isolated voltages supplied to A_1 and A_2 may be overridden with external voltages greater than the internal supply voltages. These two features of 3656 provide a great deal of versatility in possible isolation and power supply hook-ups. When external supplies are applied, the rectifying diodes (D_1 through D_4) are reverse biased and the internal voltage sources are decoupled from the amplifiers (see Figure 1). Note that when external supplies are used, they must never be lower than the internal supply voltage.

Three-Port

The power supply connections in Figure 2 show the full three-port isolation configuration. The system has three separate grounds with no galvanic connections between them. The two external 0.47µF capacitors at pins 12 and 16 filter the rectified isolated voltage at the output stage. Filtering on the input stage is provided by internal capacitors. In this configuration continuous isolation voltage ratings are: 3500V between pins 3 and 17; 3500V between pins 3 and 19; 1000V between pins 17 and 19.

Two-Port Bipolar Supply

Figure 3 shows two-port isolation which uses an external bipolar supply with its common connected to the output stage ground (pin 17). One of the supplies (either + or – could be used) provides power to the pulse generator (pins 19 and 20). The same sort of configuration is possible with the external supplies connected to the input stage. With the connection shown, filtering at pins 12 and 16 is not required. In this configuration continuous isolation voltage rating is: 3500VDC between pins 3 and 17; not applicable between pins 17 and 19; 3500VDC between pins 3 and 19.

Two-Port Single Supply

Figure 4 demonstrates two-port isolation using a single polarity supply connected to the output common (pin 17). The other polarity of supply for A_2 is internally generated (thus the filtering at pin 12). This isolated power configuration could be used at the input stage as well and either polarity of supply could be employed. In this configuration continuous isolation voltage rating is: 3500V between pins 3 and 17; 3500V between pins 3 and 19; not applicable between pins 17 and 19.

SIGNAL CONFIGURATIONS

Unity Gain Noninverting

The signal path portion of Figure 2 shows the 3656 is its simplest gain configuration: unity gain noninverting. The two 100kΩ resistors provide balanced resistances to the inverting and noninverting inputs of the amplifiers. The diode prevents latch up in case the input voltage goes more negative than the voltage at pin 4.

Noninverting With Gain

The signal path portion of Figure 3 demonstrates two additional gain configurations: gain in the output stage and noninverting gain in the input stage. The following equations apply:

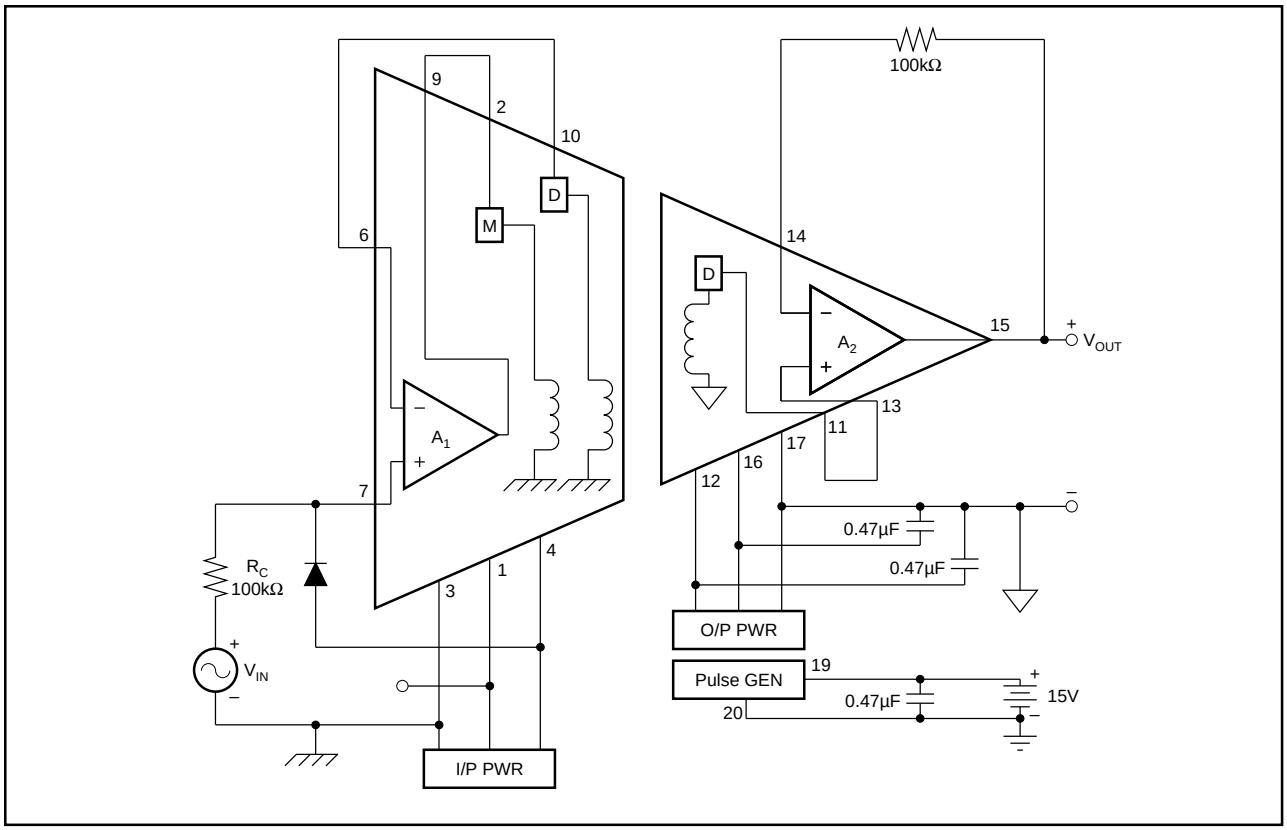


FIGURE 2. Power: Three-Port Isolation; Signal: Unity-Gain Noninverting.

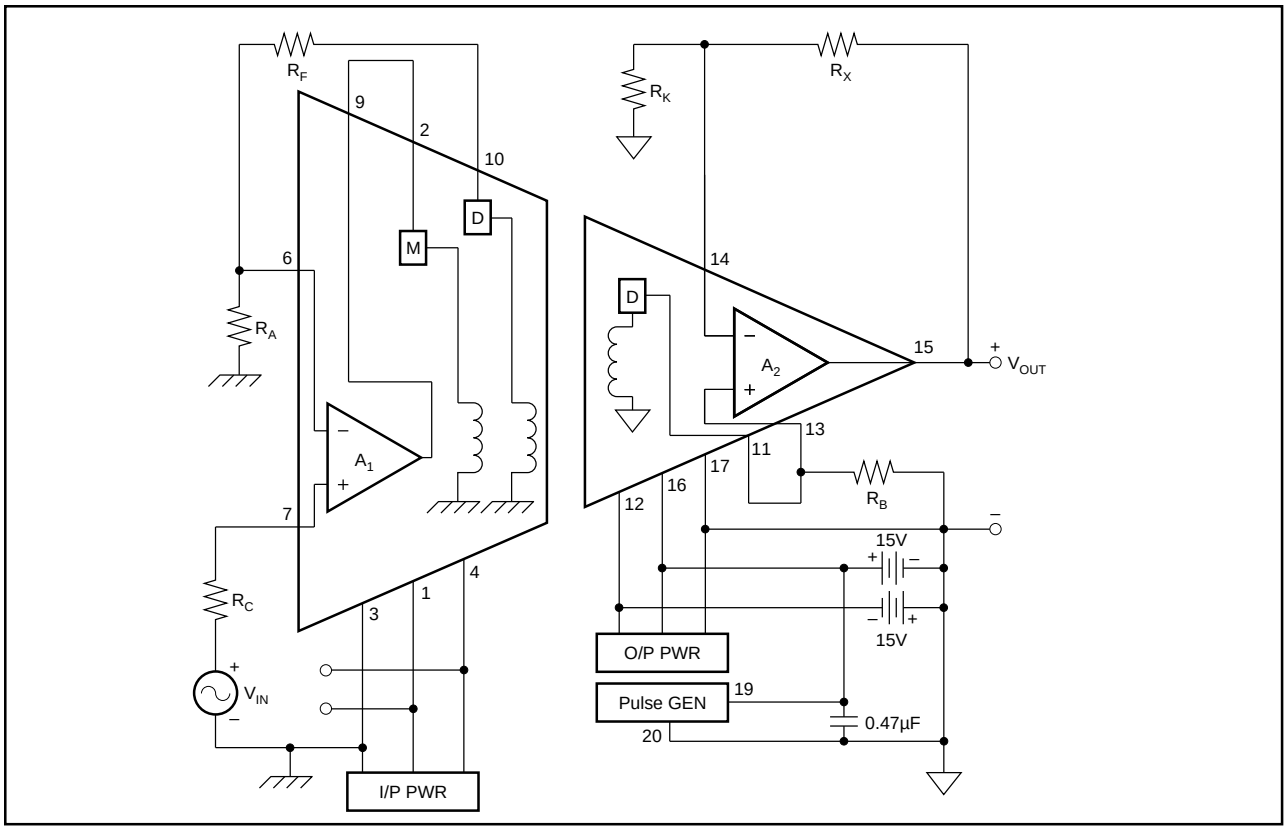


FIGURE 3. Power: Two-Port, Dual Supply; Signal: Noninverting Gain.

Total amplifier gain:

$$G = G_1 \bullet G_2 = V_{OUT}\ V_{IN} \quad (1)$$

Input Stage:

$$G_1 = 1 + (R_A/F_A) \quad (2)$$

(Select G_1 to be less than 5V/full scale V_{IN} to limit demodulator output to 5V).

$$R_A + R_F \geq 2M\Omega \quad (3)$$

(Select to load input demodulator with at least 2MΩ).

$$R_C = R_A \parallel (R_F + 100k\Omega) = \frac{R_A\,(R_F + 100k\Omega)}{R_A + R_F + 100k\Omega} \quad (4)$$

(Balance impedances seen by the + and – inputs of A_1 to reduce input offset caused by bias current).

Output Stage:

$$G_2 = 1 + (R_X/R_K) \quad (5)$$

(Select ratio to obtain V_{OUT} between 5V and 10V full scale with V_{IN} at its maximum).

$$R_X \parallel R_K = 100k\Omega \quad (6)$$

(Balance impedances seen by the + and – inputs of A_2 to reduce effect of bias current on the output offset).

$$R_B = R_A + R_F \quad (7)$$

(Load output demodulator equal to input demodulator).

Inverting Gain, Voltage or Current Input

The signal portion of Figure 4 shows two possible inverting input stage configurations: current and input, and voltage input.

Input Stage:

For the voltage input case:

$$G_1 = -R_F/R_S \quad (8)$$

(Select G_1 to be less than 5V/full scale V_{IN} to limit the demodulator output voltage to 5V).

$$R_F = 2M\Omega \quad (9)$$

(Select to load the demodulator with at least 2MΩ).

$$R_C = R_S \parallel (R_1 + 100k\Omega) = \frac{R_S\,(R_F + 100k\Omega)}{R_S + R_F + 100k\Omega} \quad (10)$$

(Balance the impedances seen by the + and– inputs of A_1).

For the current input case:

$$V_{OUT} = -I_{IN}\ R_F \bullet G_2 \quad (11)$$

$$R_C = R_F \quad (12)$$

R_F may be made larger than 2MΩ if desired. The 10pF capacitors are used to compensate for the input capacitance of A_1 and to insure frequency stability.

Output Stage:

The output stage is the same as shown in equations (5), (6), and (7).

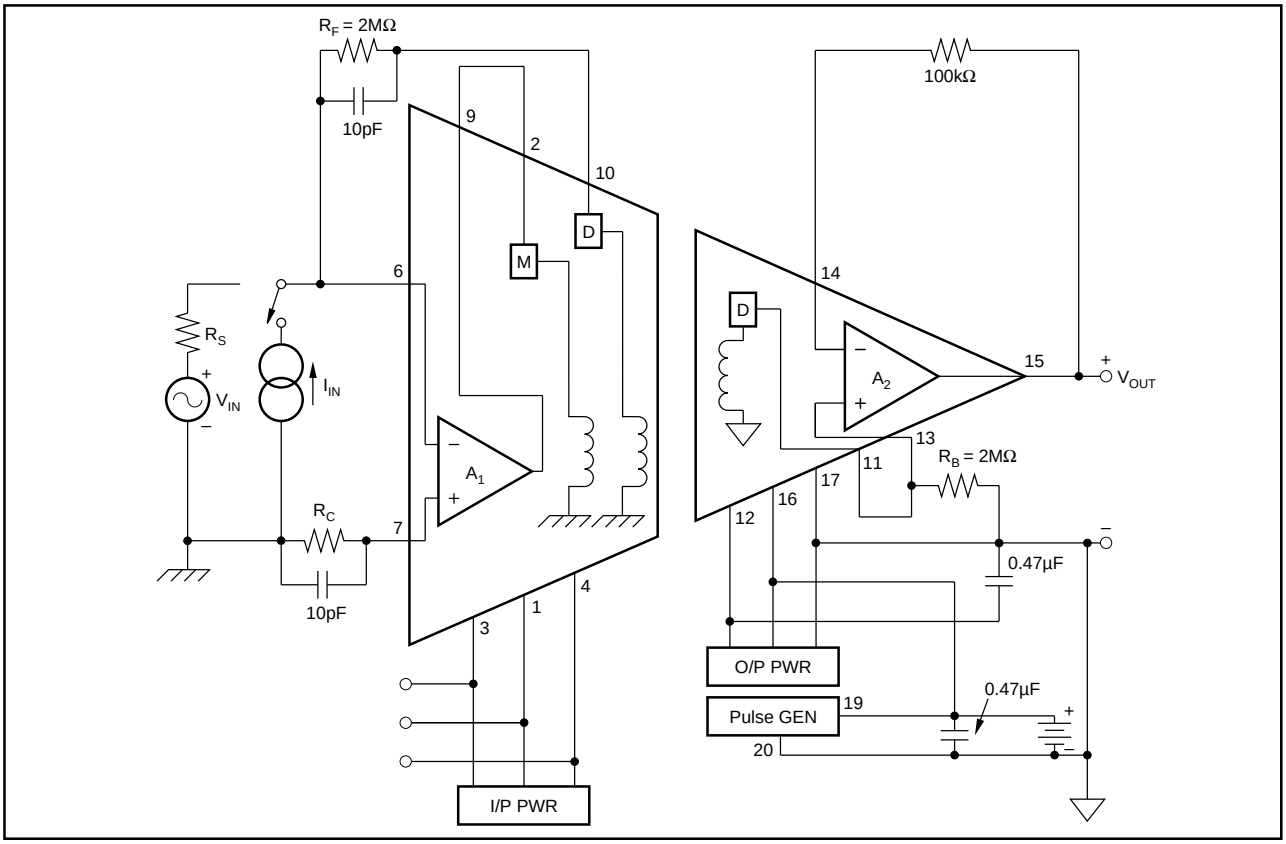


FIGURE 4. Power: Two-Port, Single Supply; Signal: Inverting Gains.

Illustrative Calculations:

The maximum input voltage is 100mV. It is desired to amplify the input signal for maximum accuracy. Noninverting output is desired.

Input Stage:

Step 1

G_1 max = 5V/max Input Signal = 5V 0.1V = 50V/V

With the above gain of 50V/V, if the input ever exceeds 100mV, it would drive the output to saturation. Therefore, it is good practice to allow reasonable input overrange.

So, to allow for 25% input overrange without saturation at the output, select:

$G_1 = 40V/V$

$G_1 = 1 + (R_F + R_A) = 40$

$\therefore R_F + R_A = 39$ (13)

Step 2

$R_A + R_F$ forms a voltage divider with the 100kΩ output resistance of the demodulator. To limit the voltage divider loading effect to no more than 5%, $R_A + R_F$ should be chosen to be at least 2MΩ. For most applications, the 2MΩ should be sufficiently large for $R_A + R_F$. Resistances greater than 2MΩ may help decrease the loading effect, but would increase the offset voltage drift.

The voltage divider with $R_A + R_F$ = 2MΩ is 2MΩ/(2MΩ + 100kΩ) = 2/(2 + 0.1) = 95.2%, i.e., the percent loading is 4.8%.

Choose $R_A + R_F = 2M\Omega$ (14)

Step 3

Solving equations (13) and (14)

$R_A = 50k\Omega$ and $R_F = 1.95M\Omega$

Step 4

The resistances seen by the + and – input terminals of the input amplifier A_1 should be closely matched in order to minimize offset voltage due to bias currents.

$\therefore R_C = R_A \parallel (R_F + 100k\Omega)$

$= 50k\Omega \parallel (1.95M\Omega + 100k\Omega)$

$\approx 49k\Omega$

Output Stage:

Step 5

$V_{OUT} = V_{IN\ MAX} \bullet G_1 \bullet G_2$

As discussed in Step 1, it is good practice to provide 25% input overrange.

So we will calculate G_2 for 10V output and 125% of the maximum input voltage.

$\therefore V_{OUT} = (1.25 \bullet 0.1)(G_1)(G_2)$

i.e., $10V = 0.125 \bullet 40 \bullet G_2$

$\therefore G_2 = 10V/5V = 2V/V$

Step 6

$G_2 = 1 + (R_X/R_K) = 2.0$

$\therefore R_X/R_K = 1.0$

$\therefore R_X = R_K$ (15)

Step 7

The resistance seen by the + input terminal of the output stage amplifier A_2 (pin 13) is the output resistance 100kΩ of the output demodulator. The resistance seen by the (–) input terminal of A_2 (pin 14) should be matched to the resistance seen by the + input terminal.

The resistance seen by pin 14 is the parallel combination of R_X and R_K.

$\therefore R_X \parallel R_K = 100k\Omega$

$(R_X \bullet R_K/(R_X + R_K) = 100k\Omega$

$R_K/[1 + (R_K/R_X)] = 100k\Omega$ (16)

Step 8

Solving equations (15) and (16) R_K = 20kΩ and R_X = 200kΩ.

Step 9

The output demodulator must be loaded equal to the input demodulator.

$\therefore R_B = R_A + R_F = 2M\Omega$

(See equation (14) above in Step 2).

Use the resistor values obtained in Steps 3, 4, 8 and 9, and connect the 3656 as shown in Figure 3.

OFFSET TRIMMING

Figure 5 shows an optional offset voltage trim circuit. It is important that $R_A + R_F = R_B$.

CASE 1: Input and output stages in low gain, use output potentiometer (R_2) only. Input potentiometer (R_1) may be disconnected. For example, unity gain could be obtained by setting $R_A = R_B = 20M\Omega$, $R_C = 100k\Omega$, $R_F = 0$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 2: Input stage in high gain and output stage in low gain, use input potentiometer (R_1) only. Output potentiometer (R_2) may be disconnected. For example, G_T = 100 could be obtained by setting $R_F = 2M\Omega$, $R_B = 2M\Omega$ returned to pin 17, $R_A = 20k\Omega$, $R_X = 100k\Omega$, and $R_K = \infty$.

CASE 3: When it is necessary to perform a two-stage precision trim (to maintain a very small offset change under conditions of changing temperature and changing gain in A_1 and A_2), use step 1 to adjust the input stage and step 2 for the output stage. Carbon composition resistors are acceptable, but potentiometers should be stable.

Step 1: Input stage trim ($R_A = R_C = 20k\Omega$, $R_I = R_B = 20M\Omega$. $R_X = 100k\Omega$, $R_K = \infty$, R_2 disconnected); A_1 high, A_2 low gain. Adjust R_1 for 0V ±5mV or desired setting at V_{OUT}, pin 15.

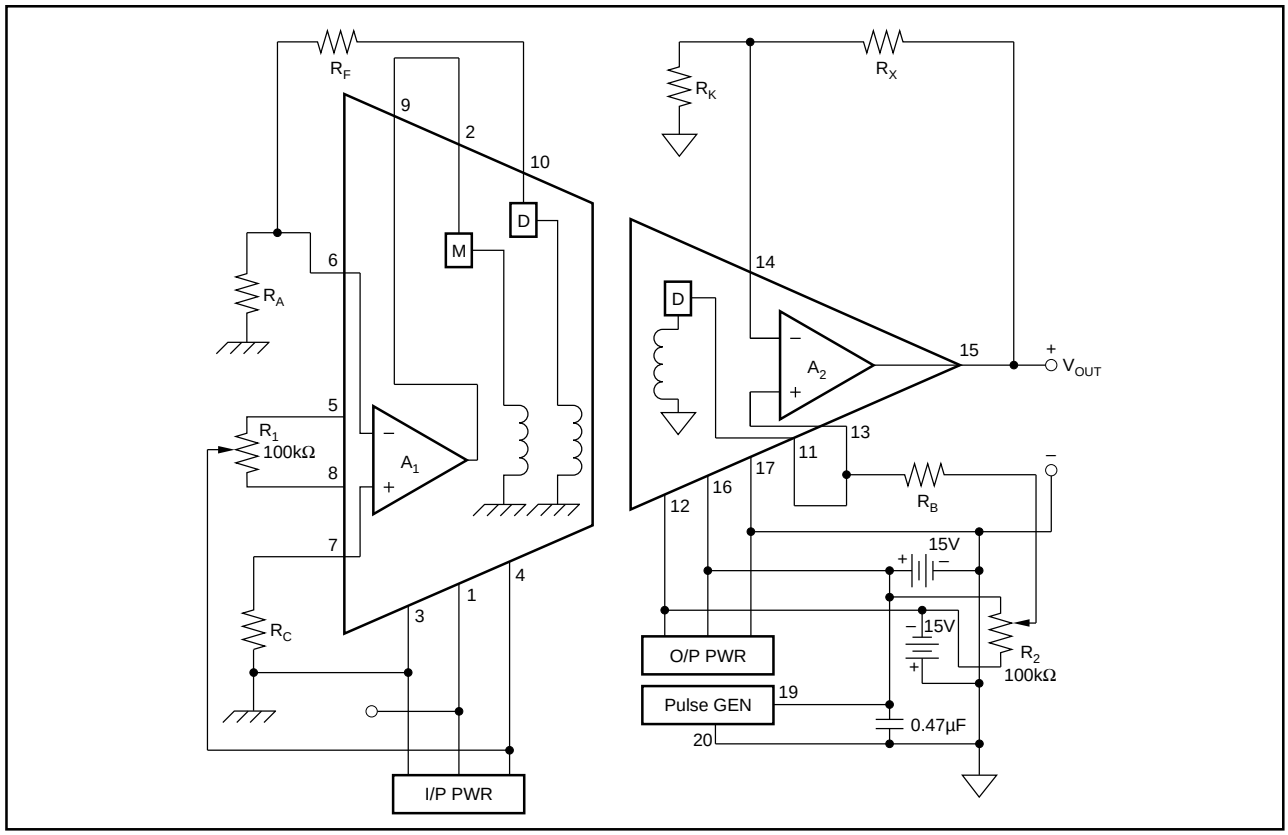


FIGURE 5. Optional Offset Voltage Trim.

Step 2: Output stage trim (R_A = R_B = 20MΩ, R_C = 100kΩ, R_F = 0, R_X = 100kΩ, R_K = ∞, R_1 and R_2 connected); A_1 low, A_2 low gain. Adjust R_2 for 0V ±1mV or desired setting at V_{OUT}, pin 15 (±110mV approximate total range).

NOTE: Other circuit component values can be used with valid results.

APPLICATIONS

ECG AMPLIFIER

Although the features of the circuit shown in Figure 6 are important in patient monitoring applications, they may also be useful in other applications. The input circuitry uses an external, low quiescent current op amp (OPA177 type) powered by the isolated power of the input stage to form a high impedance instrumentation amplifier input (true three-wire input). R_3 and R_4 give the input stage amplifier of the 3656 a noninverting gain of 10 and an inverting gain of –9. R_1 and R_2 give the external amplifier a noninverting gain of 1 + 1/9. The inputs are applied to the noninverting inputs of the two amplifiers and the composite input stage amplifier has a gain of 10.

The 330kΩ, 1W, carbon resistors and diodes D_1 - D_4 provide protection for the input amplifiers from defibrillation pulses.

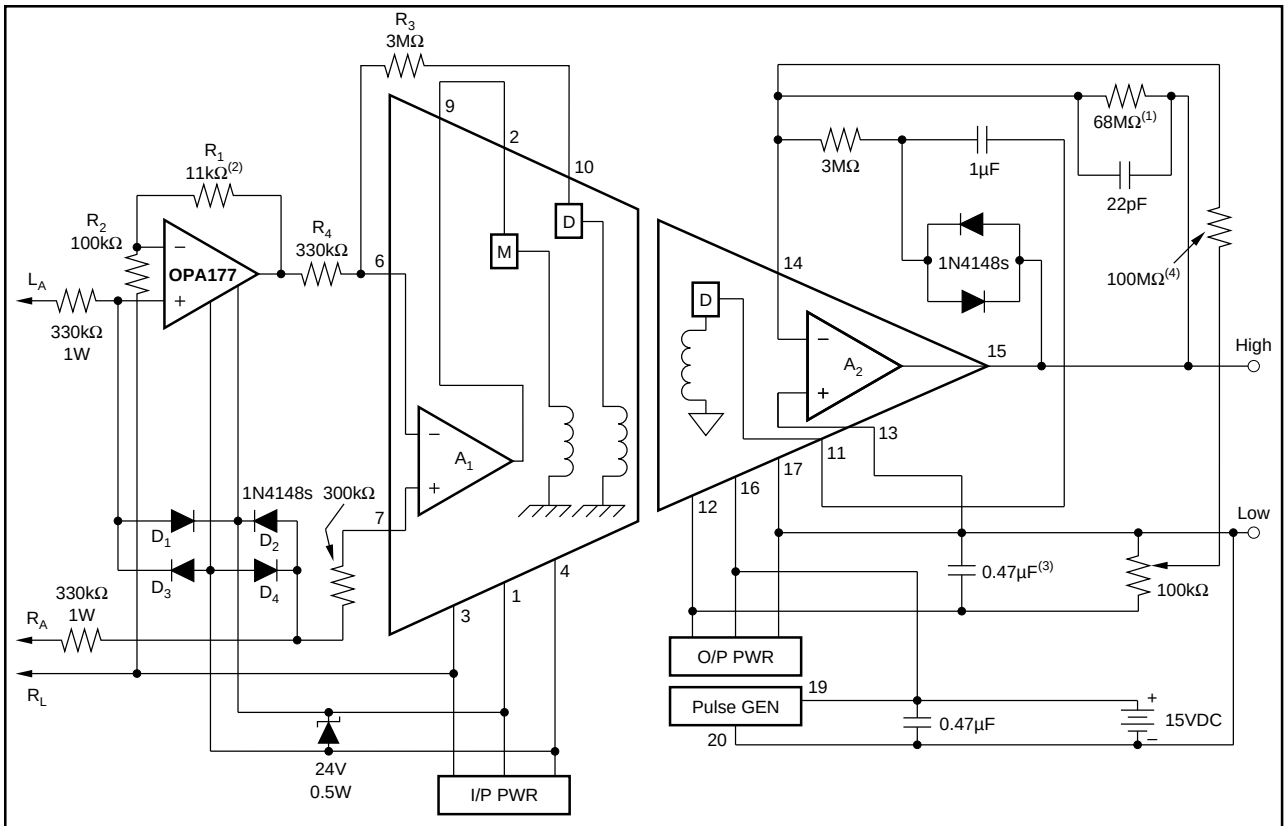
The output stage in Figure 6 is configured to provide a bandpass filter with a gain of 22.7 (68MΩ/3MΩ). The high-pass section (0.05Hz cutoff) is formed by the 1µF capacitor and 3MΩ resistor which are connected in series between the output demodulator and the inverting input of the output stage amplifier. The low-pass section (100Hz cutoff) is formed by the 68MΩ resistor and 22pF capacitor located in the feedback loop of the output stage. The diodes provide for quick recovery of the high-pass filter to overvoltages at the input. The 100kΩ pot and the 100MΩ resistor allow the output voltage to be trimmed to compensate for increased offset voltage caused by unbalanced impedances seen by the inputs of the output stage amplifier.

In many modern electrocardiographic systems, the patient is not grounded. Instead, the right-leg electrode is connected to the output of an auxiliary operational amplifier as shown in Figure 7. In this circuit, the common-mode voltage on the body is sensed by the two averaging resistors, R_1 and R_2, inverted, amplified, and fed back to the right-leg through resistor R_4. This negative feedback drives the common-mode voltage to a low value. The body's displacement current i_d does not flow to ground, but rather to the output circuit of A_3. This reduces the pickup as far as the ECG amplifier is concerned and effectively grounds the patient.

The value of R_4 should be as large as practical to isolate the patient from ground. The resistors R_3 and R_4 may be selected by these equations:

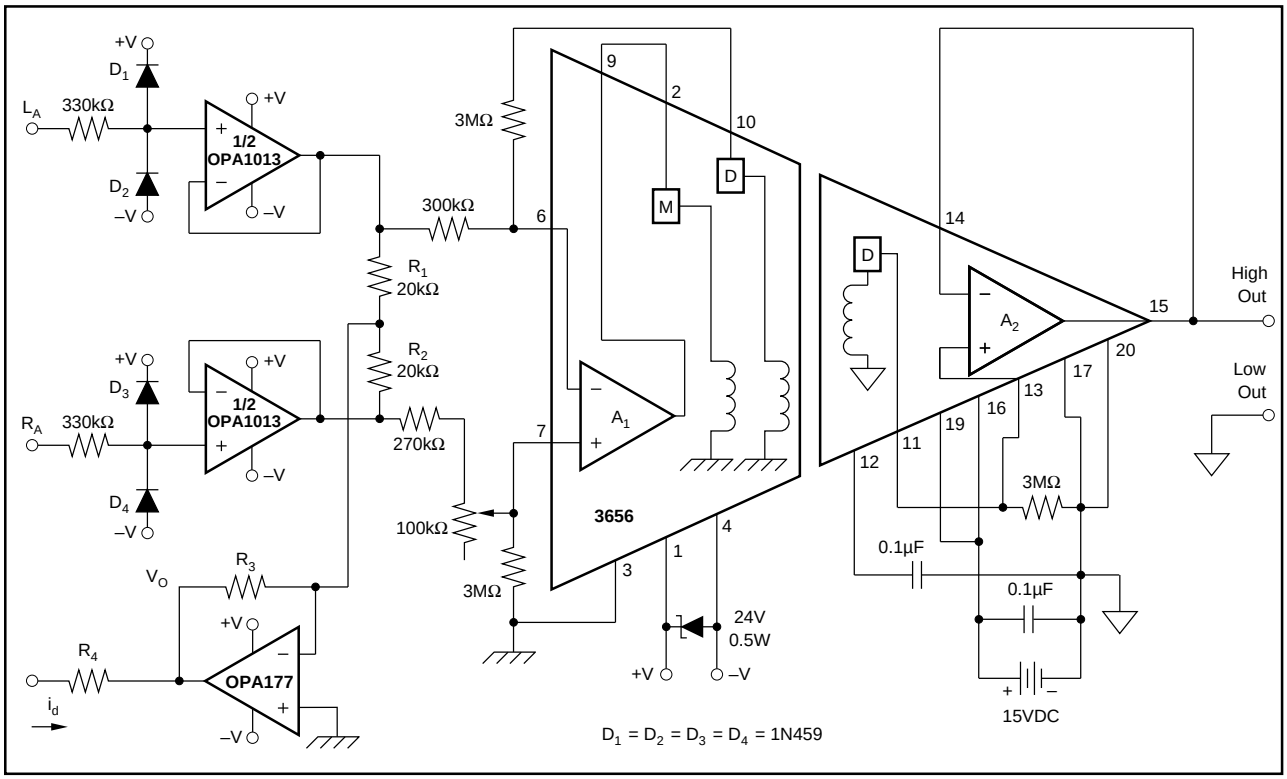
$$R_3 = (R_1/2)\ (V_O/V_{CM}) \text{ and } R_4 = (V_{CM} - V_O)/i_d$$

$$(-10V \leq V_O \leq +10V \text{ and } -10V \leq V_{CM} \leq +10V)$$



NOTES: (1) Bandpass 0.05Hz to 100Hz. (2) Adjustable resistor may be used to achieve max common-mode rejection between L_A /R_A and RL.(3) Negative 15V supply may be connected in place of 0.47µF capacitor if available. (4) See offset trimming section.

FIGURE 6. ECG Amplifier.



$D_1 = D_2 = D_3 = D_4 = 1N459$

FIGURE 7. Driven Right-Leg Amplifier.

where V_O is the output voltage of A_3, and V_{CM} is the common-mode voltage between the inputs L_A and R_A and the input common at pin 3 of the 3656.

This circuit has the added benefit of having higher common-mode rejection than the circuit in Figure 6 (approximately 10dB improvement).

BIPOLAR CURRENT OUTPUT

The three-port capability of the 3656 can be used to implement a current output isolation amplifier function—usually difficult to implement when grounded loads are involved. The circuit is shown in Figure 8 and the following equations apply:

$$G = I_{OUT}/V_{IN} = 1 + \frac{R_F}{R_A} \times \frac{R_2}{(R_1 + R_2) \bullet R_S}$$

$I_{OUT} \leq \pm 2.5mA$

$V_1 \leq \pm 4V$ (compliance)

$R_L \leq 1.6k\Omega$

$R_F + R_A = R_1 + R_2 \leq 2M\Omega$

CURRENT OUTPUT— LARGER UNIPOLAR CURRENTS

A more practical version of the current output function is shown in Figure 9. If the circuit is powered from a source greater than 15V as shown, a three-terminal regulator should be used to provide 15V for the pulse generator (pins 19 and 20). The input stage is configured as a unity gain buffer, although other configurations such as current input could be used. The circuit uses the isolation feature between the output stage and the primary power supply to generate the output current configuration that can work into a grounded load. Note that the output transistors can only drive positive current into the load. Bipolar current output would require a second transistor and dual supply.

ISOLATED 4mA TO 20mA OUTPUT

Figure 10 shows the circuit of an expanded version of the isolated current output function. It allows any input voltage range to generate the 4mA to 20mA output excursion and is also capable of zero suppression. The "span" (gain) is adjusted by R_2 and the "zero" (4mA output for minimum input) is set by the 200kΩ pot in the output stage. A three-terminal 5V reference is used to provide a stable 4mA operating point. The reference is connected to insert an adjustable bias between the demodulator output and the noninverting input of the output stage.

DIFFERENTIAL INPUT

Figure 11 shows the proper connections for differential input configuration. The 3656 is capable of operating in this input configuration only for floating loads (i.e., the source V_{IN} has no connection to the ground reference established at pin 3). For this configuration the usual 2MΩ resistor used in

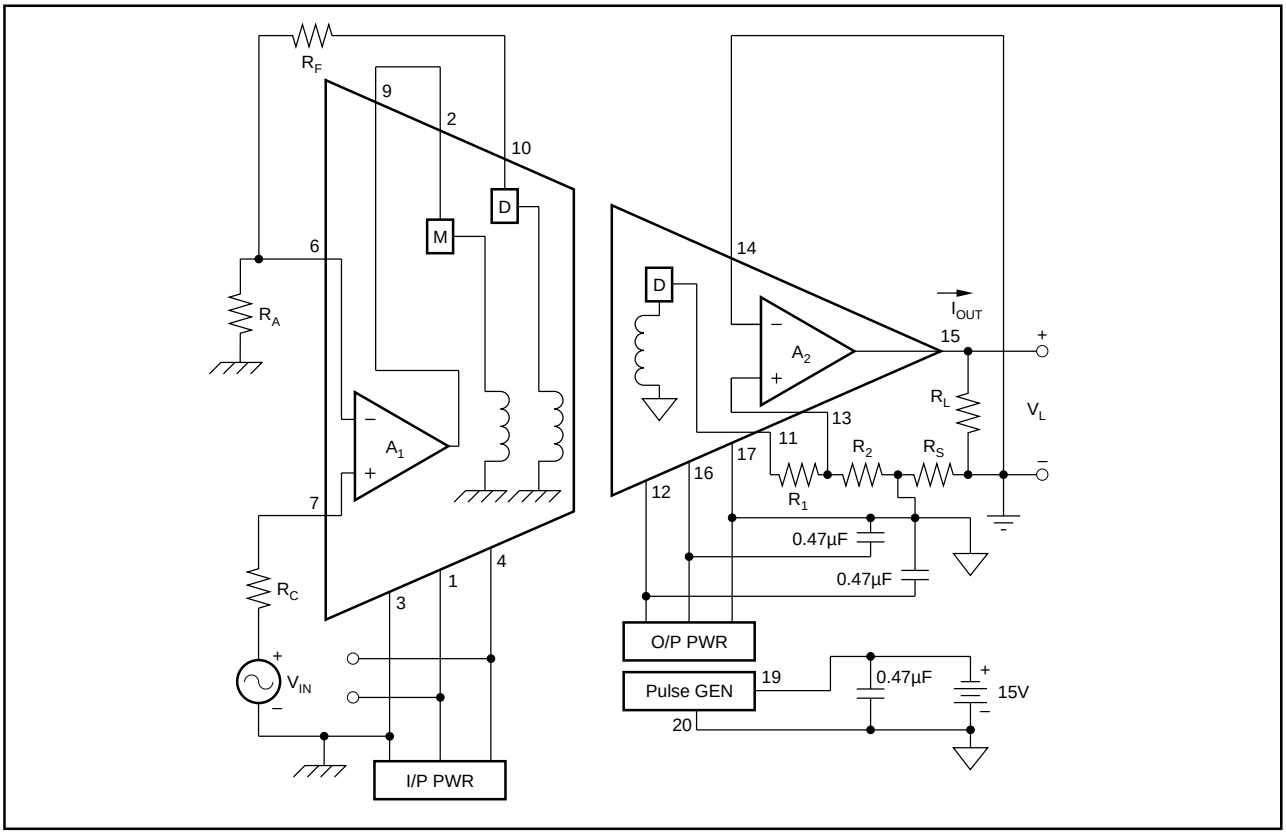


FIGURE 8. Bipolar Current Output.

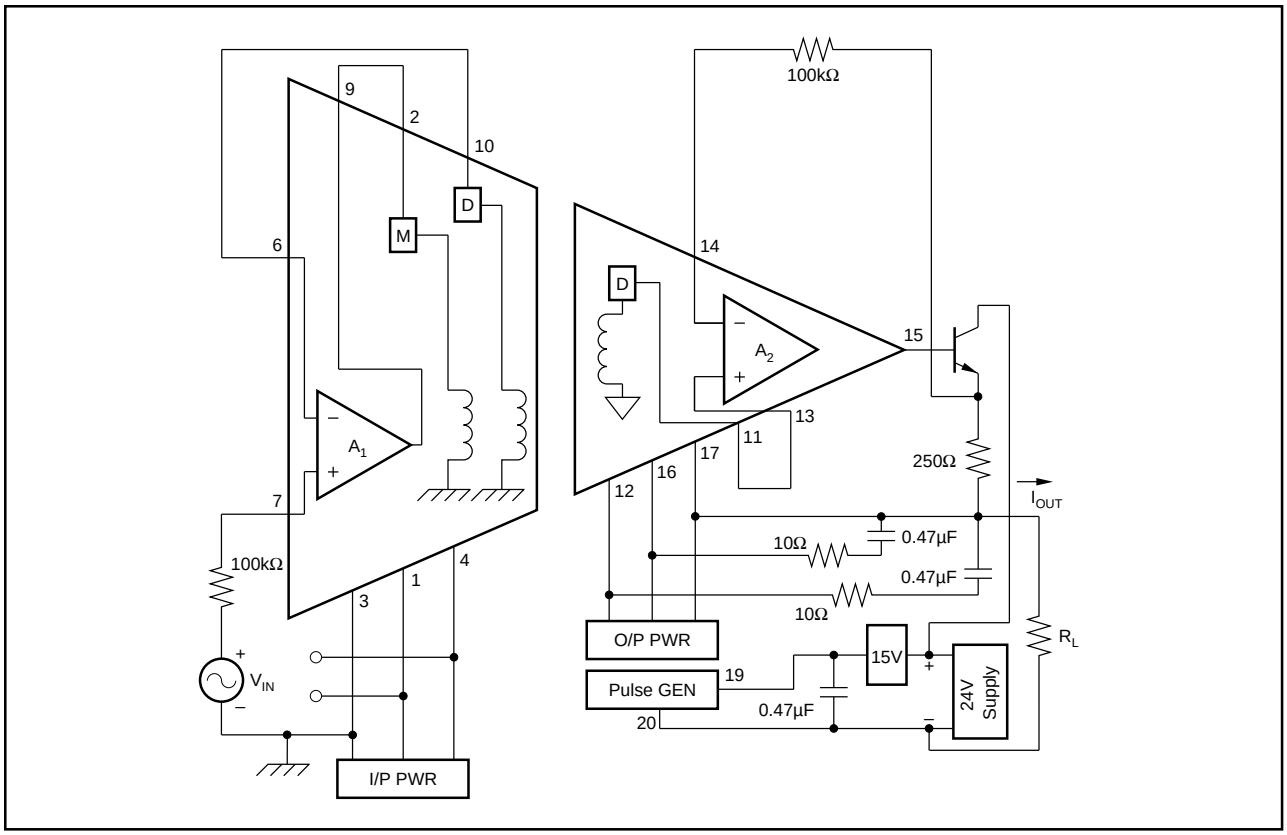


FIGURE 9. Isolated 1 to $5V_{IN}$/ 4mA to 20mA I_{OUT}.

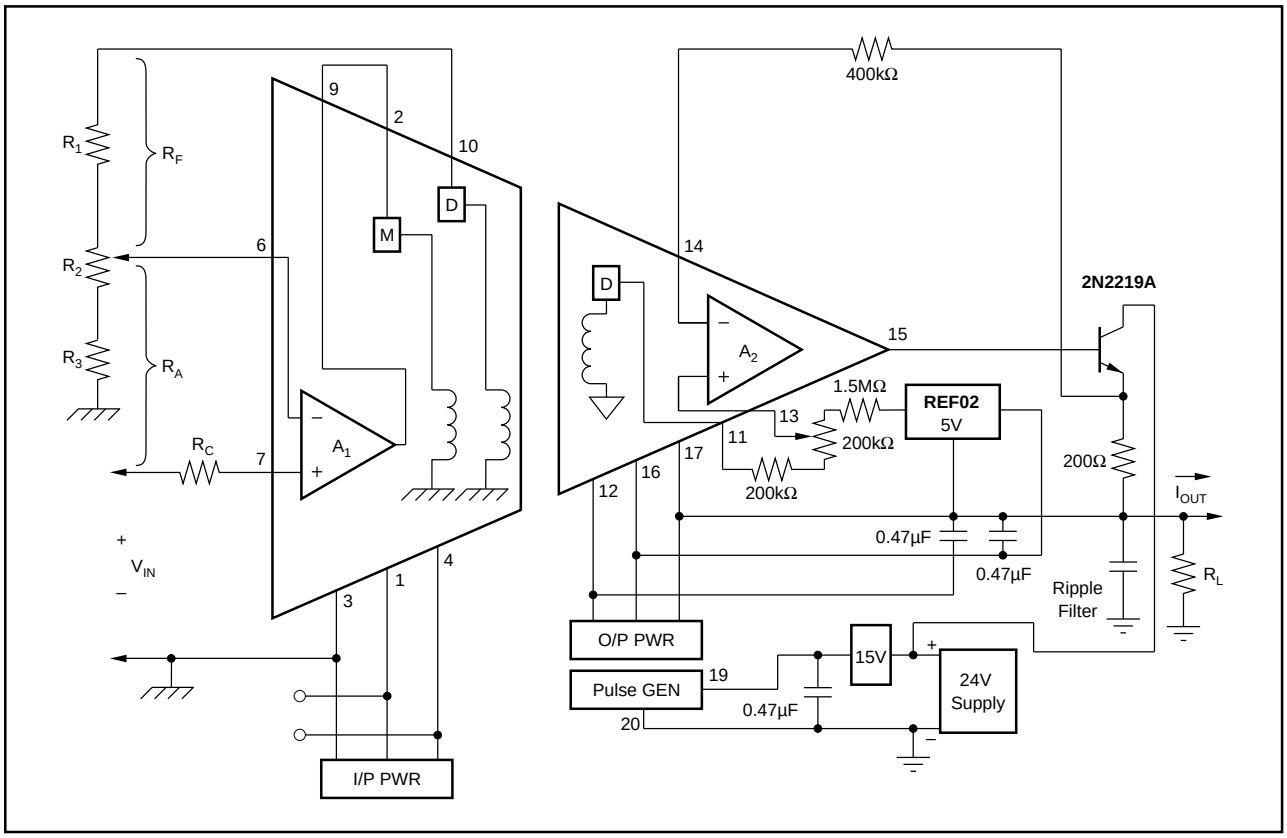


FIGURE 10. Isolated 4mA to 20mA I_{OUT}.

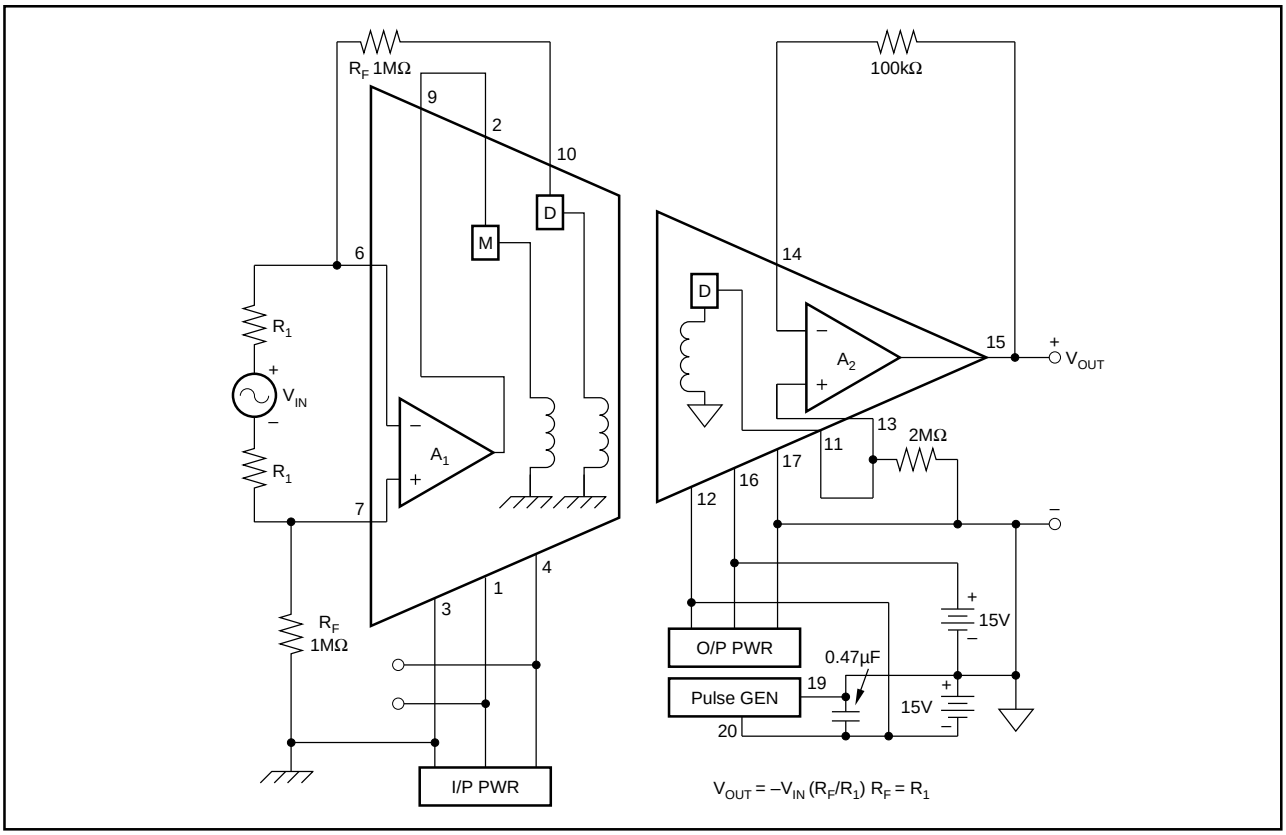


FIGURE 11. Differential Input, Floating Source.

the input stage is split into two halves, R_F and R_{F-}. The demodulator load (seen by pin 10 with respect to pin 3) is still 2MΩ for the floating load as shown. Notice pin 19 is common in Figure 11 whereas pin 20 is common in previous figures.

SERIES STRING SOURCE

Figure 12 shows a situation where a small voltage, which is part of a series string of other voltages, must be measured. The basic problem is that the small voltage to be measured is 500V above the system ground (i.e., a system common-mode voltage of 500V exists). The circuit converts this system CMV to an amplifier isolation mode voltage. Thus, the isolation voltage ratings and isolation-mode rejection specifications apply.

IMPROVED INPUT CHARACTERISTICS

In situations where it is desired to have better DC input amplifier characteristics than the 3656 normally provides, it is possible to add a precision operational amplifier as shown in Figure 13. Here the instrumentation grade OPA177 is supplied from the isolated power of the input stage. The 3656 is configured as a unity-gain buffer. The gain of the OPA177 stage must be chosen to limit its full scale output voltage to 5V and avoid overdriving the 3656's demodulators. Since the 3656 draws a significant amount of supply current, extra filtering or the input supply is required as shown (2 x 0.47µF).

ELECTROMAGNETIC RADIATION

The transformer coupling used in 3656 for isolation makes the 3656 a source of electromagnetic radiation unless it is properly shielded. Physical separation between the 3656 and sensitive components may not give sufficient attenuation by itself. In these applications, the use of an electromagnetic shield is a must. A shield, Burr-Brown 100MS, is specially designed for use with the 3656 package. Note that the offset voltage appearing at pin 15 may change by 4mV to 12mV with use of the shield; however, this can be trimmed (see Offset Trimming section).

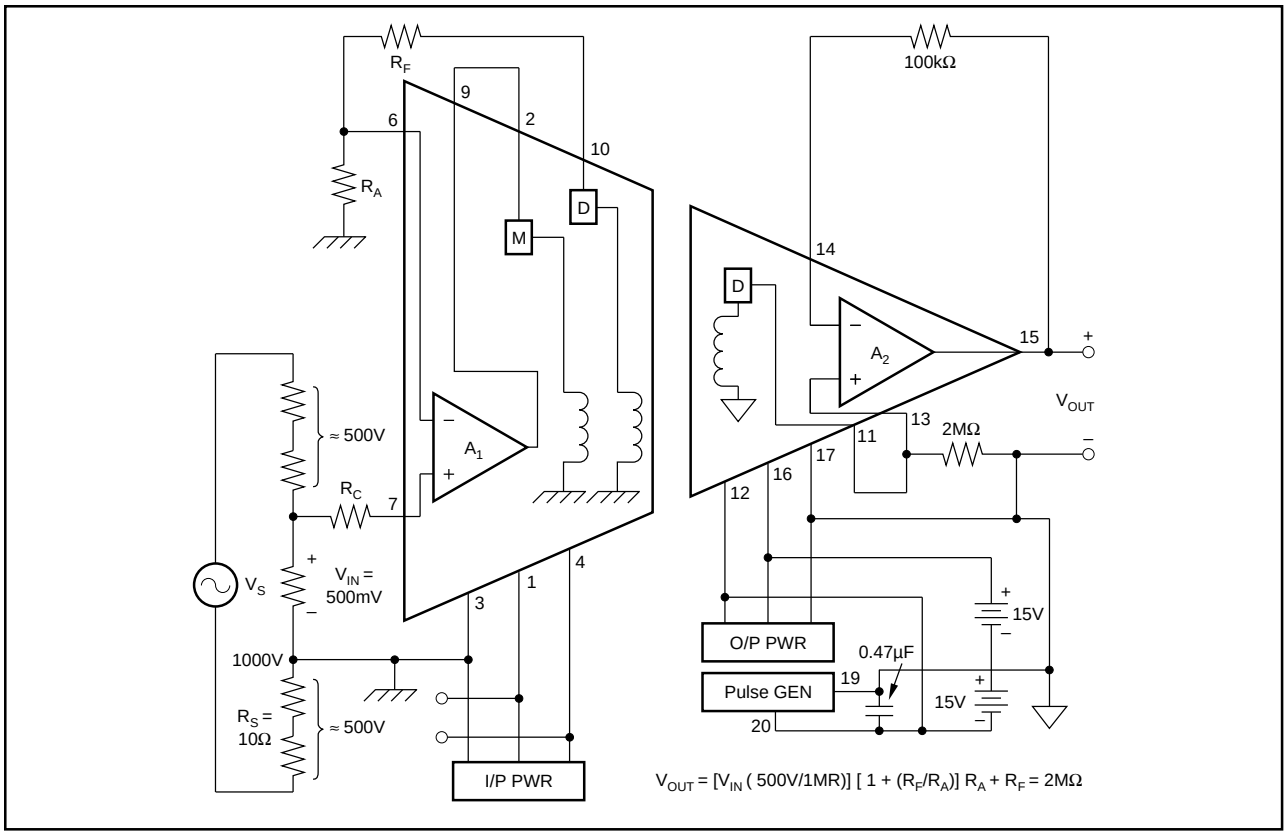


FIGURE 12. Series Source.

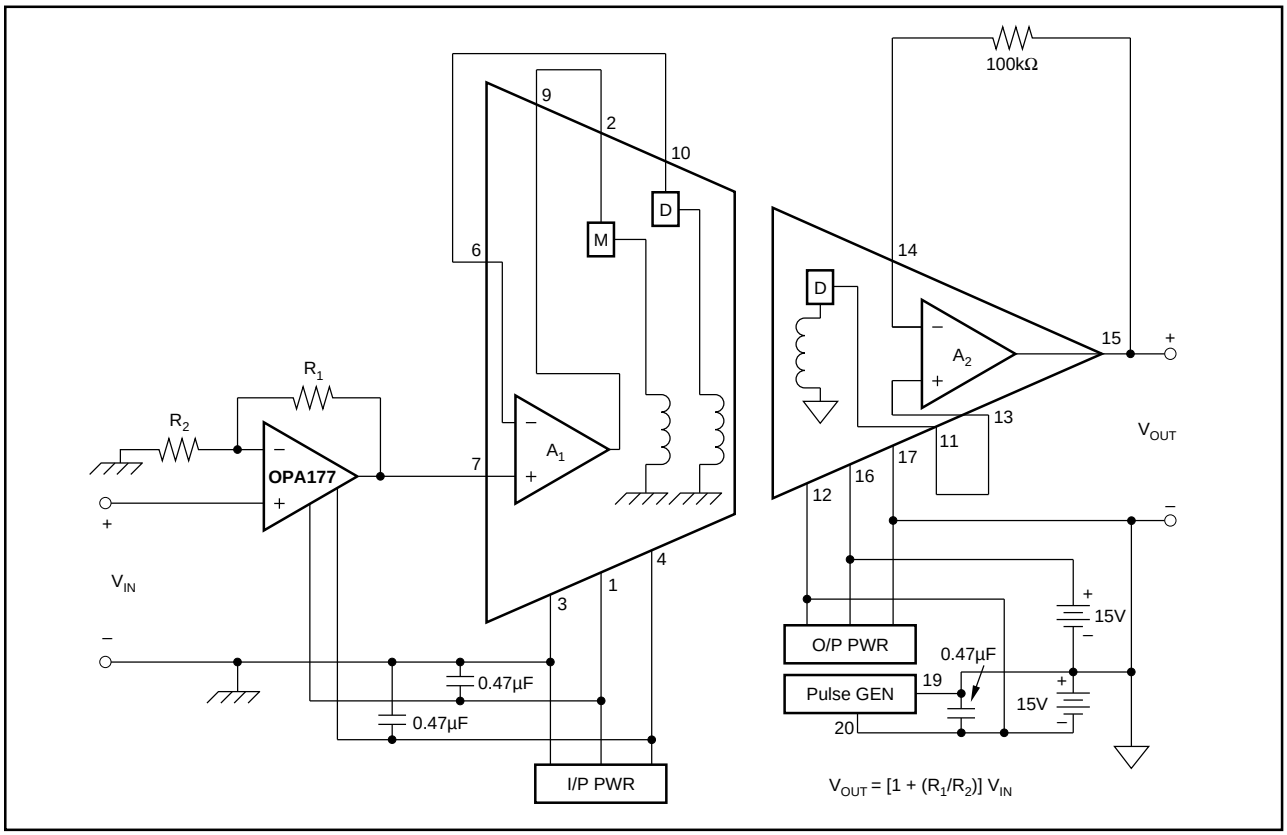


FIGURE 13. Isolator for Low-Level Signals.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
3656AG	OBSOLETE	CDIP	JND	20		TBD	Call TI	Call TI	Samples Not Available
3656BG	OBSOLETE	CDIP	JND	20		TBD	Call TI	Call TI	Samples Not Available
3656HG	OBSOLETE	CDIP	JND	20		TBD	Call TI	Call TI	Samples Not Available
3656JG	OBSOLETE	CDIP	JND	20		TBD	Call TI	Call TI	Samples Not Available
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(1) The marketing status values are defined as follows:
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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