

Overview

The 32 Bit RIMM[®] Continuity module is a blank module designed to be inserted into any unused 32 Bit RIMM socket in a RDRAM[®] memory subsystem. There are no active components on the continuity module. The Continuity module is used to connect the RDRAM Channel signal traces through unused RIMM connectors so that the Rambus electrical signals may be properly terminated on the Continuity module.

The RDRAM Architecture enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed, memory transactions. The use of Rambus Signaling Level (RSL) technology permits 800MHz and 1066MHz data transfer rates while using conventional system and PCB design technologies. The separate control and data buses with independent row and column control yield over 95% bus efficiency.

Related Documentation

Datasheets for RDRAM memory system components are available on the web at www.rDRAM.com. Check the RDRAM website regularly for the latest document.

Features

- 232 edge connector pads with 1mm pad spacing
- Used with 1066 and 800MHz RDRAM memory subsystems
- Maximum 32 Bit RIMM continuity module PCB size: 133.5mm x 31.75mm x 1.37mm (5.25" x 1.25" x 0.054")
- Gold plated edge connector pad contacts
- No active components
- Suitable for use with 232 contact RIMM Connectors
- 28Ω Typical Module Impedance
- Terminated channel is terminated by 28Ω resistors to Vterm

Form Factor

The 32 Bit RIMM Continuity modules are offered in 232-pad 1mm edge connector pad pitch suitable for 232 contact RIMM connectors.

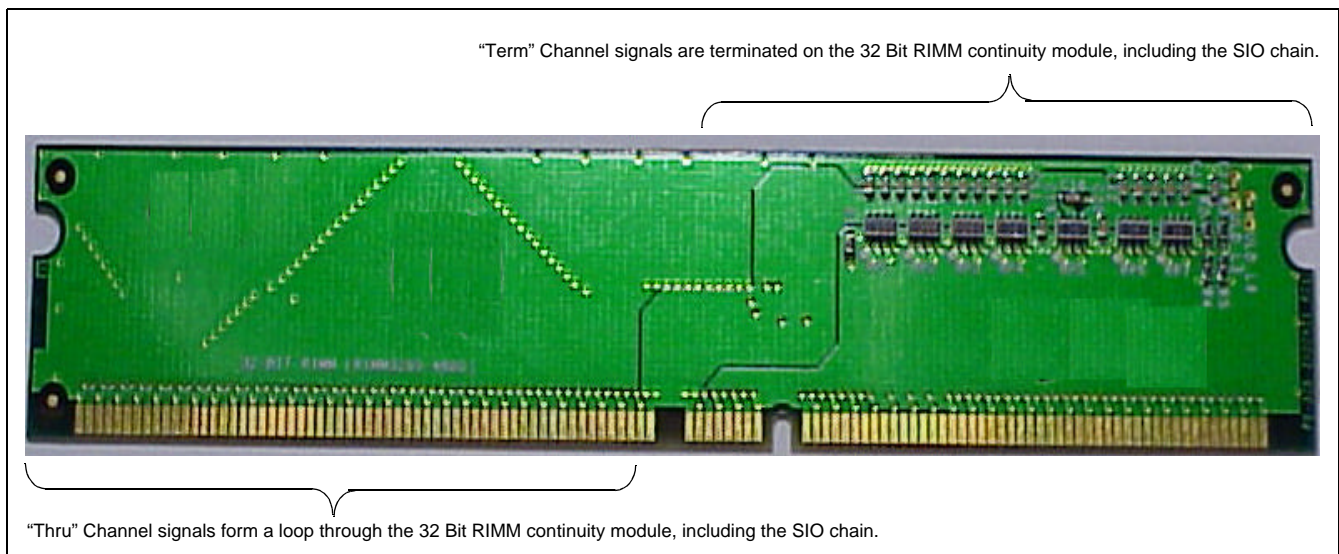


Figure 1: 32 Bit RIMM Continuity Module

Table 1: Module Pad Numbers and Signal Names

| Pad | Signal Name | Pad | Signal Name |
|-----|-------------|-----|-------------|
| A1 | Gnd | B1 | Gnd |
| A2 | SCK_THRU_L | B2 | CMD_THRU_L |
| A3 | Gnd | B3 | Gnd |
| A4 | DQA8_THRU_L | B4 | DQA7_THRU_L |
| A5 | Gnd | B5 | Gnd |
| A6 | DQA6_THRU_L | B6 | DQA5_THRU_L |
| A7 | Gnd | B7 | Gnd |
| A8 | DQA4_THRU_L | B8 | DQA3_THRU_L |
| A9 | Gnd | B9 | Gnd |
| A10 | DQA2_THRU_L | B10 | DQA1_THRU_L |
| A11 | Gnd | B11 | Gnd |
| A12 | DQA0_THRU_L | B12 | CTMN_THRU_L |
| A13 | Gnd | B13 | Gnd |
| A14 | CFM_THRU_L | B14 | CTM_THRU_L |
| A15 | Gnd | B15 | Gnd |
| A16 | CFMN_THRU_L | B16 | ROW2_THRU_L |
| A17 | Gnd | B17 | Gnd |
| A18 | ROW1_THRU_L | B18 | ROW0_THRU_L |
| A19 | Gnd | B19 | Gnd |
| A20 | COL4_THRU_L | B20 | COL3_THRU_L |
| A21 | Gnd | B21 | Gnd |
| A22 | COL2_THRU_L | B22 | COL1_THRU_L |
| A23 | Gnd | B23 | Gnd |
| A24 | COL0_THRU_L | B24 | DQB0_THRU_L |
| A25 | Gnd | B25 | Gnd |
| A26 | DQB1_THRU_L | B26 | DQB2_THRU_L |
| A27 | Gnd | B27 | Gnd |
| A28 | DQB3_THRU_L | B28 | DQB4_THRU_L |
| A29 | Gnd | B29 | Gnd |
| A30 | DQB5_THRU_L | B30 | DQB6_THRU_L |
| A31 | Gnd | B31 | Gnd |
| A32 | DQB7_THRU_L | B32 | DQB8_THRU_L |
| A33 | Gnd | B33 | Gnd |
| A34 | SOUT_THRU | B34 | SIN_THRU |
| A35 | Gnd | B35 | Gnd |
| A36 | DQB8_THRU_R | B36 | DQB7_THRU_R |
| A37 | Gnd | B37 | Gnd |
| A38 | DQB6_THRU_R | B38 | DQB5_THRU_R |
| A39 | Gnd | B39 | Gnd |
| A40 | DQB4_THRU_R | B40 | DQB3_THRU_R |
| A41 | Gnd | B41 | Gnd |
| A42 | DQB2_THRU_R | B42 | DQB1_THRU_R |
| A43 | Gnd | B43 | Gnd |
| A44 | DQB0_THRU_R | B44 | COL0_THRU_R |
| A45 | Gnd | B45 | Gnd |

| Pad | Signal Name | Pad | Signal Name |
|------|-------------|------|-------------|
| A59 | Gnd | B59 | Gnd |
| A60 | Vterm | B60 | Vterm |
| A61 | Vterm | B61 | Vterm |
| A62 | Gnd | B62 | Gnd |
| A63 | DQA3_THRU_R | B63 | DQA4_THRU_R |
| A64 | Gnd | B64 | Gnd |
| A65 | DQA5_THRU_R | B65 | DQA6_THRU_R |
| A66 | Gnd | B66 | Gnd |
| A67 | DQA7_THRU_R | B67 | DQA8_THRU_R |
| A68 | Gnd | B68 | Gnd |
| A69 | Vdd | B69 | Vdd |
| A70 | Gnd | B70 | Gnd |
| A71 | SCK_THRU_R | B71 | CTMN_TERM_L |
| A72 | Gnd | B72 | Gnd |
| A73 | CMD_THRU_R | B73 | CTM_TERM_L |
| A74 | Gnd | B74 | Gnd |
| A75 | Vref | B75 | Vcmos |
| A76 | Vdd | B76 | Vdd |
| A77 | SVdd | B77 | SWP |
| A78 | Vdd | B78 | Vdd |
| A79 | SCL | B79 | SDA |
| A80 | Vdd | B80 | Vdd |
| A81 | SA0 | B81 | SA1 |
| A82 | Vdd | B82 | Vdd |
| A83 | SA2 | B83 | SIN_TERM |
| A84 | Gnd | B84 | Gnd |
| A85 | DQB8_TERM | B85 | DQB7_TERM |
| A86 | Gnd | B86 | Gnd |
| A87 | DQB6_TERM | B87 | DQB5_TERM |
| A88 | Gnd | B88 | Gnd |
| A89 | DQB4_TERM | B89 | DQB3_TERM |
| A90 | Gnd | B90 | Gnd |
| A91 | DQB2_TERM | B91 | DQB1_TERM |
| A92 | Gnd | B92 | Gnd |
| A93 | DQB0_TERM | B93 | COL0_TERM |
| A94 | Gnd | B94 | Gnd |
| A95 | COL1_TERM | B95 | COL2_TERM |
| A96 | Gnd | B96 | Gnd |
| A97 | COL3_TERM | B97 | COL4_TERM |
| A98 | Gnd | B98 | Gnd |
| A99 | ROW0_TERM | B99 | ROW1_TERM |
| A100 | Gnd | B100 | Gnd |
| A101 | ROW2_TERM | B101 | CFMN_TERM |
| A102 | Gnd | B102 | Gnd |
| A103 | CTM_TERM_R | B103 | CFM_TERM |

Table 1: Module Pad Numbers and Signal Names (Continued)

| Pad | Signal Name | Pad | Signal Name |
|-----|-------------|-----|-------------|
| A46 | COL1_THRU_R | B46 | COL2_THRU_R |
| A47 | Gnd | B47 | Gnd |
| A48 | COL3_THRU_R | B48 | COL4_THRU_R |
| A49 | Gnd | B49 | Gnd |
| A50 | ROW0_THRU_R | B50 | ROW1_THRU_R |
| A51 | Gnd | B51 | Gnd |
| A52 | ROW2_THRU_R | B52 | CFMN_THRU_R |
| A53 | Gnd | B53 | Gnd |
| A54 | CTM_THRU_R | B54 | CFM_THRU_R |
| A55 | Gnd | B55 | Gnd |
| A56 | CTMN_THRU_R | B56 | DQA0_THRU_R |
| A57 | Gnd | B57 | Gnd |
| A58 | DQA1_THRU_R | B58 | DQA2_THRU_R |

| Pad | Signal Name | Pad | Signal Name |
|------|-------------|------|-------------|
| A104 | Gnd | B104 | Gnd |
| A105 | CTMN_TERM_R | B105 | DQA0_TERM |
| A106 | Gnd | B106 | Gnd |
| A107 | DQA1_TERM | B107 | DQA2_TERM |
| A108 | Gnd | B108 | Gnd |
| A109 | DQA3_TERM | B109 | DQA4_TERM |
| A110 | Gnd | B110 | Gnd |
| A111 | DQA5_TERM | B111 | DQA6_TERM |
| A112 | Gnd | B112 | Gnd |
| A113 | DQA7_TERM | B113 | DQA8_TERM |
| A114 | Gnd | B114 | Gnd |
| A115 | CMD_TERM | B115 | SCK_TERM |
| A116 | Gnd | B116 | Gnd |

AC Electrical Specifications

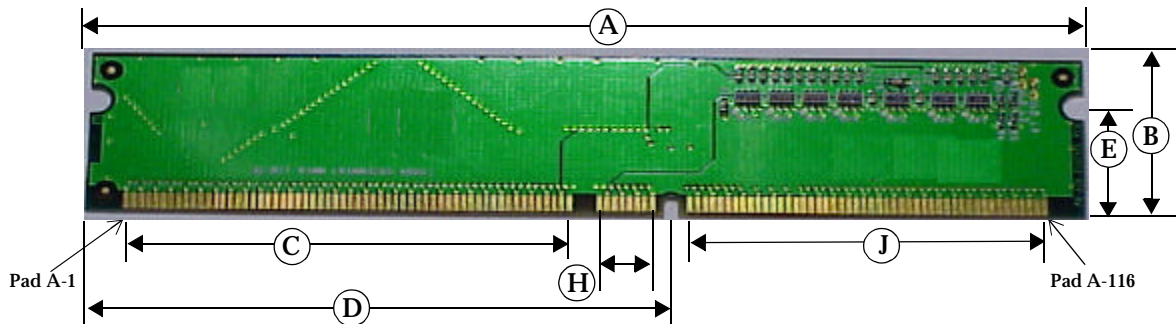
| Symbol | Parameter and Conditions | Min | Typ | Max | Unit |
|-------------------------|---|------|-----|------|----------|
| Z_L | Channel impedance | 25.2 | 28 | 30.8 | Ω |
| $Z_{UL-CMOS}$ | Module impedance of SCK and CMD signals | 23.8 | 28 | 32.2 | Ω |
| T_{PD} | Average RSL clock delay ^a | - | - | 0.88 | ns |
| ΔT_{PD} | Propagation delay variation of RSL signals with respect to T_{PD} ^a | -20 | - | 20 | ps |
| $\Delta T_{PD-CMOS}$ | Propagation delay variation of SCK signal with respect to an average clock delay ^a | -250 | - | 250 | ps |
| $\Delta T_{PD-SCK,CMD}$ | Propagation delay variation of CMD signal with respect to SCK signal | -200 | - | 200 | ps |
| V_{α}/V_{IN} | Attenuation Limit | - | - | 10 | % |
| V_{XF}/V_{IN} | Forward crosstalk coefficient (300ps input signal rise time @ 20%-80%) | - | - | 3 | % |
| V_{XB}/V_{IN} | Backward crosstalk coefficient (300ps input signal rise time @ 20%-80%) | - | - | 1.25 | % |
| R_{DC} | DC Resistance | - | - | 0.5 | Ω |

a. T_{PD} or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).

Physical Dimensions

There are only passive components mounted on the top side of the module.

Figure 2 defines the 32 Bit RIMM Continuity module dimensions. All units are in millimeters/inches.



| Dimension | Description | Min | Nom | Max | Unit |
|-----------|---|-----------------|-----------------|-----------------|----------|
| A | PCB length | 133.20 5.244 | 133.35 5.250 | 133.50 5.256 | mm in |
| B | PCB height | - | - | 31.750 1.250 | mm in |
| C | Center-center pad width from pads A1 to A60, B1 to B60 | - | 59.00 2.323 | - | mm in |
| D | Spacing from PCB left edge to connector key notch | 78.100 3.075 | 78.175 3.078 | 78.250 3.081 | mm in |
| E | Spacing from contact pad PCB edge to side edge retainer notch | - | 17.780 0.700 | - | mm in |
| F | PCB thickness | 1.170 0.046 | 1.270 0.050 | 1.370 0.054 | mm in |
| H | Center-center pad width from pad A61 to A68, B61 to B68 | - | 7.00 0.276 | - | mm in |
| J | Center-center pad width from pad A69 to A116, B69 to B116 | - | 47.00 1.850 | - | mm in |

Figure 2: 32 Bit RIMM Continuity Module PCB Physical Description

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Document DL0201 Version 0.9

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