



3-Volt Advanced+ Boot Block Flash Memory

28F800C3, 28F160C3, 28F320C3, 28F640C3 (x16)

Preliminary Datasheet

Product Features

- Flexible SmartVoltage Technology
 - 2.7 V–3.6 V Read/Program/Erase
 - 12 V for Fast Production Programming
- 1.65 V–2.5 V or 2.7 V–3.6 V I/O Option
 - Reduces Overall System Power
- High Performance
 - 2.7 V–3.6 V: 70 ns Max Access Time
- Optimized Architecture for Code Plus Data Storage
 - Eight 4-Kword Blocks, Top or Bottom Locations
 - Up to One Hundred-Twenty-Seven 32-Kword Blocks
 - Fast Program Suspend Capability
 - Fast Erase Suspend Capability
- Flexible Block Locking
 - Lock/Unlock Any Block
 - Full Protection on Power-Up
 - WP# Pin for Hardware Block Protection
 - $V_{PP} = GND$ Option
 - V_{CC} Lockout Voltage
- Low Power Consumption
 - 9 mA Typical Read Power
 - 7 μA Typical Standby Power with Automatic Power Savings Feature
- 12 V Fast Production Program
- Extended Temperature Operation
 - -40 °C to +85 °C
- 128-bit Protection Register
 - 64-bit Unique Device Identifier
 - 64-bit User Programmable OTP Cells
- Extended Cycling Capability
 - Minimum 100,000 Block Erase Cycles
- Supports Intel® Flash Data Integrator Software
 - Flash Memory Manager
 - System Interrupt Manager
 - Supports Parameter Storage, Streaming Data (e.g., voice)
- Automated Word/Byte Program and Block Erase
 - Command User Interface
 - Status Registers
- Cross-Compatible Command Support
 - Intel Basic Command Set
 - Common Flash Interface
- Standard Surface Mount Packaging
 - 48-Ball CSP Packages
 - 64-Ball Easy BGA Packages
 - 48-Lead TSOP Package
- ETOX™ VIII (0.13 μm) Flash Technology
 - 32- and 64-Mbit
- ETOX™ VII (0.18 μm) Flash Technology
 - 16-, 32-, 64-Mbit
- ETOX™ VI (0.25 μm) Flash Technology
 - 8-, 16- and 32-Mbit

The 3-Volt Advanced+ Boot Block Flash memory, manufactured on Intel's latest 0.13 μm and 0.18 μm technologies, represents a feature-rich solution for low-power applications. 3-Volt Advanced+ Boot Block Flash memory devices incorporate low-voltage capability (2.7 V read, program and erase) with high-speed, low-power operation. Flexible block locking allows any

Notice: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.



block to be independently locked or unlocked. Add to this the Intel® Flash Data Integrator (IFDI) software and you have a cost-effective, flexible, monolithic code plus data storage solution. Intel® 3-Volt Advanced+ Boot Block products will be available in 48-lead TSOP, 48-ball CSP, and 64-ball Easy BGA packages. Additional information on this product family can be obtained by accessing the Intel® Flash website: <http://www.intel.com/design/flash>.

Information in this document is provided in connection with Intel® products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The 28F800C3, 28F160C3, 28F320C3, 28F640C3 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

Copyright © Intel Corporation, 1998 – 2001.

*Other names and brands may be claimed as the property of others.

Contents

| | | |
|------------|---|----|
| 1.0 | Introduction | 1 |
| 1.1 | Product Overview | 2 |
| 2.0 | Product Description | 3 |
| 2.1 | Package Pinouts | 3 |
| 2.2 | Block Organization | 9 |
| 2.2.1 | Parameter Blocks | 9 |
| 2.2.2 | Main Blocks | 9 |
| 3.0 | Principles of Operation | 9 |
| 3.1 | Bus Operation | 9 |
| 3.1.1 | Read | 9 |
| 3.1.2 | Output Disable | 10 |
| 3.1.3 | Standby | 10 |
| 3.1.4 | Reset | 10 |
| 3.1.5 | Write | 11 |
| 3.2 | Modes of Operation | 11 |
| 3.2.1 | Read Array | 11 |
| 3.2.2 | Read Configuration | 12 |
| 3.2.3 | Read Status Register | 12 |
| 3.2.4 | Read Query | 13 |
| 3.2.5 | Program Mode | 13 |
| 3.2.6 | Erase Mode | 14 |
| 3.3 | Flexible Block Locking | 17 |
| 3.3.1 | Locking Operation | 18 |
| 3.3.2 | Unlocked State | 18 |
| 3.3.3 | Lock-Down State | 18 |
| 3.3.4 | Reading Block-Lock Status | 19 |
| 3.3.5 | Locking Operations during Erase Suspend | 19 |
| 3.3.6 | Status Register Error Checking | 19 |
| 3.4 | 128-Bit Protection Register | 20 |
| 3.4.1 | Reading the Protection Register | 20 |
| 3.4.2 | Programming the Protection Register | 21 |
| 3.4.3 | Locking the Protection Register | 21 |
| 3.5 | V _{PP} Program and Erase Voltages | 21 |
| 3.5.1 | Improved 12-Volt Production Programming | 21 |
| 3.5.2 | V _{PP} & V _{PPLK} for Complete Protection | 22 |
| 3.6 | Power Consumption | 22 |
| 3.6.1 | Active Power (Program/Erase/Read) | 23 |
| 3.6.2 | Automatic Power Savings (APS) | 23 |
| 3.6.3 | Standby Power | 23 |
| 3.6.4 | Deep Power-Down Mode | 23 |
| 3.7 | Power-Up/Down Operation | 23 |
| 3.7.1 | RP# Connected to System Reset | 24 |
| 3.7.2 | VCC, VPP and RP# Transitions | 24 |
| 3.8 | Power Supply Decoupling | 24 |



| | | |
|------------|---|----|
| 4.0 | Electrical Specifications | 25 |
| 4.1 | Absolute Maximum Ratings | 25 |
| 4.2 | Operating Conditions | 26 |
| 4.3 | Capacitance | 26 |
| 4.4 | DC Characteristics | 27 |
| 4.5 | AC Characteristics—Read Operations..... | 31 |
| 4.6 | AC Characteristics—Write Operations..... | 36 |
| 4.7 | Erase and Program Timings | 40 |
| 4.8 | Reset Operations | 42 |
| 5.0 | Ordering Information | 43 |
| 6.0 | Additional Information | 45 |
| A | WSM Current/Next States, Sheet 1 of 2 | 46 |
| B | Program/Erase Flowcharts | 48 |
| C | Common Flash Interface Query Structure | 54 |
| D | Architecture Block Diagram | 61 |
| E | Word-Wide Memory Map Diagrams | 62 |
| F | Device ID Table | 66 |
| G | Protection Register Addressing | 67 |

Revision History

| Date of Revision | Version | Description |
|------------------|---------|--|
| 05/12/98 | -001 | Original version |
| 07/21/98 | -002 | 48-Lead TSOP package diagram change μ BGA package diagrams change 32-Mbit ordering information change (Section 6) CFI Query Structure Output Table Change (Table C2) CFI Primary-Vendor Specific Extended Query Table Change for Optional Features and Command Support change (Table C8) Protection Register Address Change I_{PPD} test conditions clarification (Section 4.3) μ BGA package top side mark information clarification (Section 6) |
| 10/03/98 | -003 | Byte-Wide Protection Register Address change V_{IH} Specification change (Section 4.3) V_{IL} Maximum Specification change (Section 4.3) I_{CCS} test conditions clarification (Section 4.3) Added Command Sequence Error Note (Table 7) Datasheet renamed from <i>3 Volt Advanced Boot Block, 8-, 16-, 32-Mbit Flash Memory Family</i> . |
| 12/04/98 | -004 | Added t_{BHWL}/t_{BHEH} and t_{QVBL} (Section 4.6) Programming the Protection Register clarification (Section 3.4.2) |
| 12/31/98 | -005 | Removed all references to x8 configurations |
| 02/24/99 | -006 | Removed reference to 40-Lead TSOP from front page |
| 06/10/99 | -007 | Added Easy BGA package (Section 1.2) Removed 1.8 V I/O references <i>Locking Operations Flowchart</i> changed (Appendix B) Added t_{WHGL} (Section 4.6) CFI Primary Vendor-Specific Extended Query changed (Appendix C) |
| 03/20/00 | -008 | Max I_{CCD} changed to 25 μ A Table 10, added note indicating $V_{CCMax} = 3.3$ V for 32-Mbit device |
| 04/24/00 | -009 | Added specifications for 0.18 micron product offerings throughout document Added 64-Mbit density |
| 10/12/00 | -010 | Changed references of 32Mbit 80ns devices to 70ns devices to reflect the faster product offering. Changed $V_{CCMax}=3.3V$ reference to indicate that the affected product is the 0.25 μ m 32Mbit device. Minor text edits throughout document. |
| 7/20/01 | -011 | Added 1.8v I/O operation documentation where applicable Added TSOP PCN 'Pin-1' indicator information Changed references in 8 x 8 BGA pinout diagrams from 'GND' to 'Vssq' Added 'Vssq' to Pin Descriptions Information Removed 0.4 μ m references in DC characteristics table Corrected 64Mb package Ordering Information from 48- μ BGA to 48-VFBGA Corrected 'bottom' boot block sizes to on 8Mb device to 8 x 4KWords Minor text edits throughout document |
| 10/02/01 | -012 | Added specifications for 0.13 micron product offerings throughout document |

1.0 Introduction

This document contains the specifications for the 3-Volt Advanced+ Boot Block Flash Memory family. These flash memories add features, such as instant block locking and a protection register, that can be used to enhance the security of systems.

This family of products features 1.65 V – 2.5 V or 2.7 V–3.6 V I/Os and a low V_{CC}/V_{PP} operating range of 2.7 V–3.6 V for Read, Program, and Erase operations. In addition, this family is capable of fast programming at 12 V. Throughout this document, the term “2.7 V” refers to the full voltage range 2.7 V–3.6 V (except where noted otherwise) and “ $V_{PP} = 12 V$ ” refers to 12 V $\pm 5\%$. [Section 1.0](#) and [Section 2.0](#) provide an overview of the flash memory family including applications, pinouts, pin descriptions, and memory organization. [Section 3.0](#) describes the operation of these products, with [Section 4.0](#) providing the operating specifications. [Section 5.0](#) outlines ordering information, and [Section 6.0](#) describes the location of additional reference material.

The 3-Volt Advanced+ Boot Block flash memory features include the following:

- Zero-latency, flexible block locking
- 128-bit Protection Register
- Simple system implementation for 12-V production programming with 2.7-V, in-field programming
- Ultra low-power operation at 2.7 V
- V_{CCQ} input of 1.65 V–2.5 V on all I/Os. See Figures 1 through 4 for pinout diagrams and V_{CCQ} location
- Minimum 100,000 block erase cycles
- Common Flash Interface for software query of device specs and features

Table 1. 3-Volt Advanced+ Boot Block Feature Summary

| Feature | 8 Mbit ⁽¹⁾ , 16 Mbit, 32 Mbit ⁽²⁾ | Reference |
|----------------------------|--|----------------------------|
| V_{CC} Operating Voltage | 2.7 V – 3.6 V ⁽³⁾ | Table 8 |
| V_{PP} Voltage | Provides complete write protection with optional 12 V Fast Programming | Table 8 |
| V_{CCQ} I/O Voltage | 1.65 V – 2.5 V or 2.7 V – 3.6 V | |
| Bus Width | 16-bit | Table 2 |
| Speed (ns) | 8 Mbit: 90, 110 @ 2.7 V and 80, 100 @ 3.0 V 16 Mbit: 70, 80, 90, 110 @ 2.7 V and 70, 80, 100 @ 3.0 V 32 Mbit: 70, 90, 100, 110 @ 2.7 V and 70, 90, 100 @ 3.0 V 64 Mbit: 80, 100 @ 2.7 V and 80, 100 @ 3.0 V | Section 4.4 |
| Blocking (top or bottom) | 8 x 4-Kword parameter 8-Mb: 15 x 32-Kword main 16-Mb: 31 x 32-Kword main 32-Mb: 63 x 32-Kword main 64-Mb: 127 x 32-Kword main | Appendix 2.2 Appendix E |
| Operating Temperature | Extended: –40 °C to +85 °C | Table 8 |
| Program/Erase Cycling | 100,000 cycles | Table 8 |
| Packages | 48-Lead TSOP 48-Ball μ BGA* CSP ⁽¹⁾ , 48-Ball VF BGA, Easy BGA | Figure 1, 2 and 3 |
| Block Locking | Flexible locking of any block with zero latency | Section 3.3 |
| Protection Register | 64-bit unique device number, 64-bit user programmable | Section 3.4 |

NOTES:

1. 8-Mbit density not available in μ BGA* CSP.
2. See Specification Update for changes to 32-Mbit devices (order 297938).
3. $V_{CCMax} = 3.3$ V on 0.25 μ m 32-Mbit devices.

1.1 Product Overview

Intel provides secure low voltage memory solutions with the Advanced Boot Block family of products. A new block locking feature allows instant locking/unlocking of any block with zero latency. A 128-bit protection register allows unique flash device identification.

Discrete supply pins provide single voltage read, program, and erase capability at 2.7 V, while also allowing 12-V V_{PP} for faster production programming. Improved 12 V, a new feature designed to reduce external logic, simplifies board designs when combining 12-V production programming with 2.7-V in-field programming.

The 3-Volt Advanced+ Boot Block flash memory products are available in x16 packages in the following densities: (see [Section 5.0, “Ordering Information” on page 43](#))

- 8-Mbit (8, 388, 608 bit) flash memories organized as 512 Kwords of 16 bits each
- 16-Mbit (16, 777, 216 bit) flash memories organized as 1024 Kwords of 16 bits each
- 32-Mbit (33, 554, 432 bit) flash memories organized as 2048 Kwords of 16 bits each
- 64-Mbit (67, 108, 864 bit) flash memories organized as 4096 Kwords of 16 bits each.

Eight 4-Kword parameter blocks are located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map in order to accommodate different microprocessor protocols for kernel code location. The remaining memory is grouped into 64-Kbyte main blocks (see [Appendix E](#)).

All blocks can be locked or unlocked instantly to provide complete protection for code or data (see [Section 3.3, “Flexible Block Locking” on page 17](#) for details).

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the flash memory. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for Program and Erase operations, including verification, thereby unburdening the microprocessor or microcontroller. The status register indicates the status of the WSM by signifying block-erase or word program completion and status.

Program and erase automation allows Program and Erase operations to be executed using an industry-standard two-write command sequence to the CUI. Program operations are performed in word increments. Erase operations erase all locations within a block simultaneously. Both Program and Erase operations can be suspended by the system software in order to read from any other block. In addition, data can be programmed to another block during an erase suspend.

The 3-Volt Advanced+ Boot Block flash memories offer two low-power savings features: Automatic Power Savings (APS), and standby mode. The device automatically enters APS mode following the completion of a read cycle. Standby mode is initiated when the system deselects the device by driving CE# inactive. Combined, these two power-savings features significantly reduce power consumption.

The device can be reset by lowering RP# to GND, which provides CPU memory reset synchronization and additional protection against bus noise that may occur during system reset and power-up/down sequences (see Section 3.5 and Section 3.6).

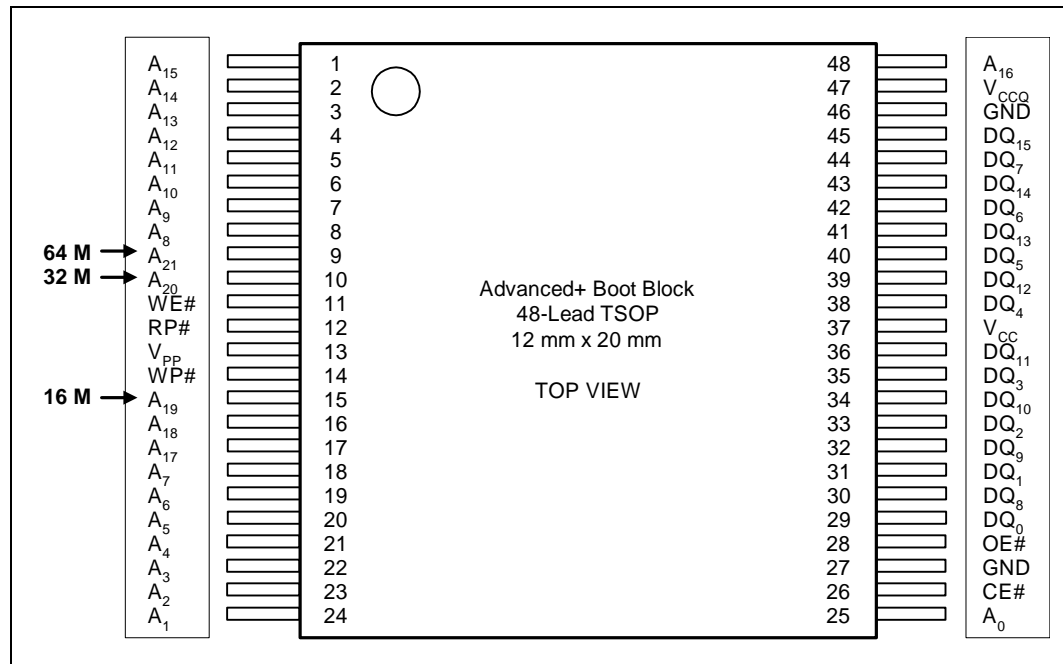
Refer to Section 4.4, “DC Characteristics” on page 27 for complete current and voltage specifications. Refer to Section 4.5 and Section 4.6 for read and write performance specifications. Section 4.7 shows program and erase times.

2.0 Product Description

This section provides device pin descriptions and package pinouts for the 3-Volt Advanced+ Boot Block Flash Memory family, which is available in 48-lead TSOP (x16) and 48-ball μ BGA and Easy BGA packages (Figures 1, 2 and 3, respectively).

2.1 Package Pinouts

Figure 1. 48-Lead TSOP Package

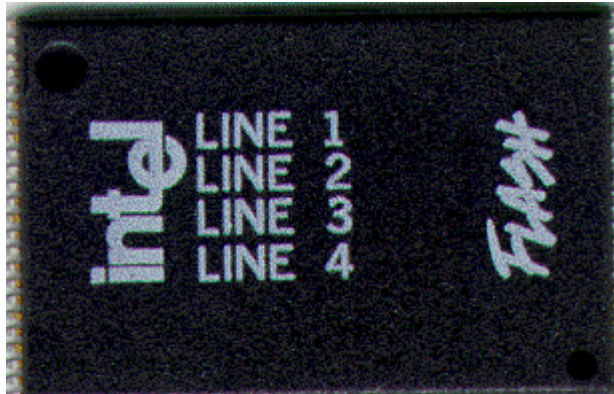


0645_02

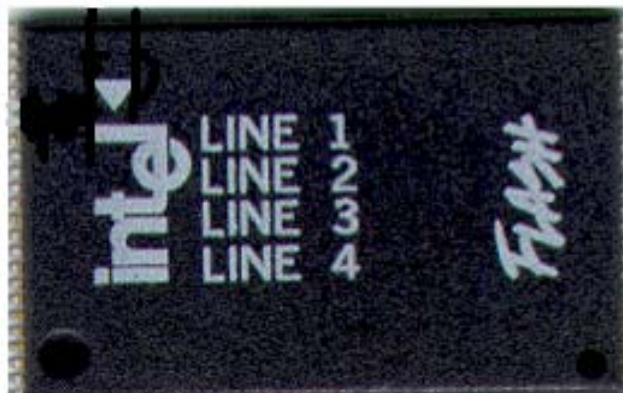
Note: Lower densities will have NC on the upper address pins. For example, a 16-Mbit device will have NC on Pins 9 and 10.

Figure 2. New Mark for Pin-1 indicator on 48-Lead 8Mb, 16Mb and 32Mb TSOP

Current Mark:



New Mark:



Note: The topside marking on 8 Mb, 16 Mb, and 32 Mb Advanced and Advanced + Boot Block 48L TSOP products will convert to a white ink triangle as a Pin 1 indicator. Products without the white triangle will continue to use a dimple as a Pin 1 indicator. There are no other changes in package

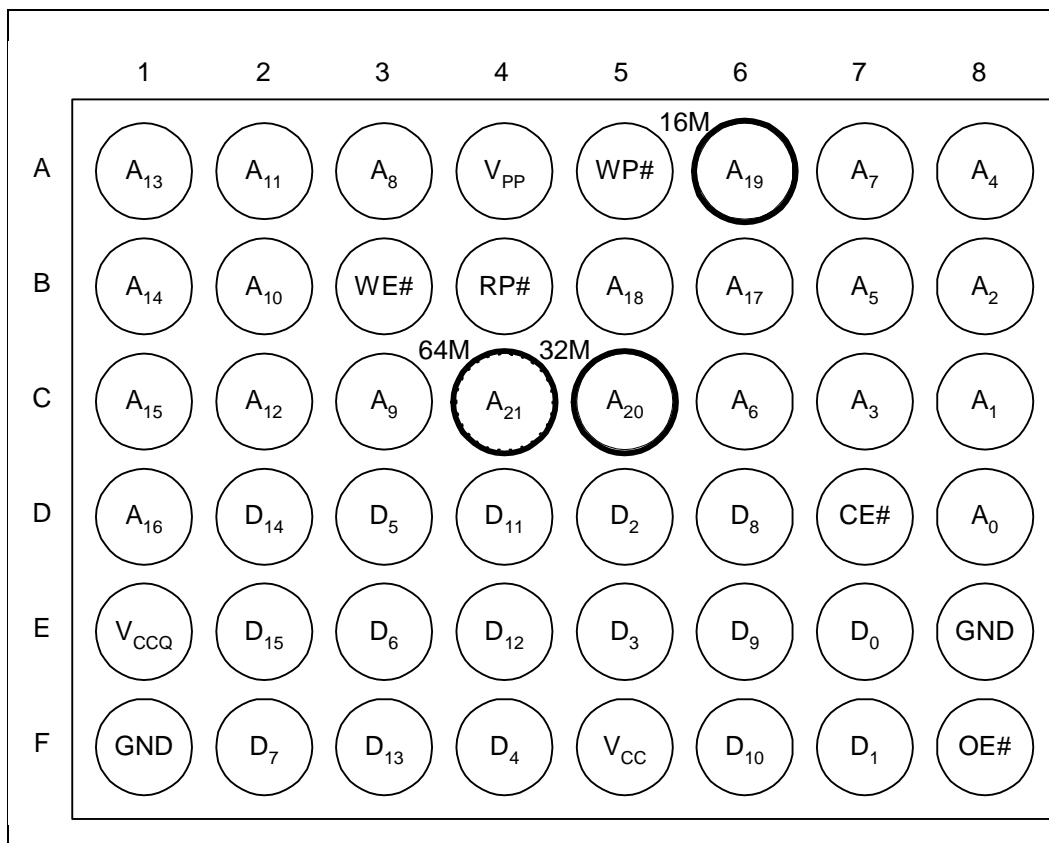


size, materials, functionality, customer handling, or manufacturability. Product will continue to meet Intel stringent quality requirements.

Products Affected are Intel Ordering Codes:

| | 48-Lead TSOP |
|-----------------------------|--|
| Extended 32 Mbit | TE28F320C3TC70 TE28F320C3BC70 TE28F320C3TC90 TE28F320C3BC90 TE28F320C3TA100 TE28F320C3BA100 TE28F320C3TA110 TE28F320C3BA110 |
| Extended 16 Mbit | TE28F160C3TC70 TE28F160C3BC70 TE28F160C3TC80 TE28F160C3BC80 TE28F160C3TA90 TE28F160C3BA90 TE28F160C3TA110 TE28F160C3BA110 |
| Extended 8 Mbit | TE28F800C3TA90 TE28F800C3BA90 TE28F800C3TA110 TE28F800C3BA110 |

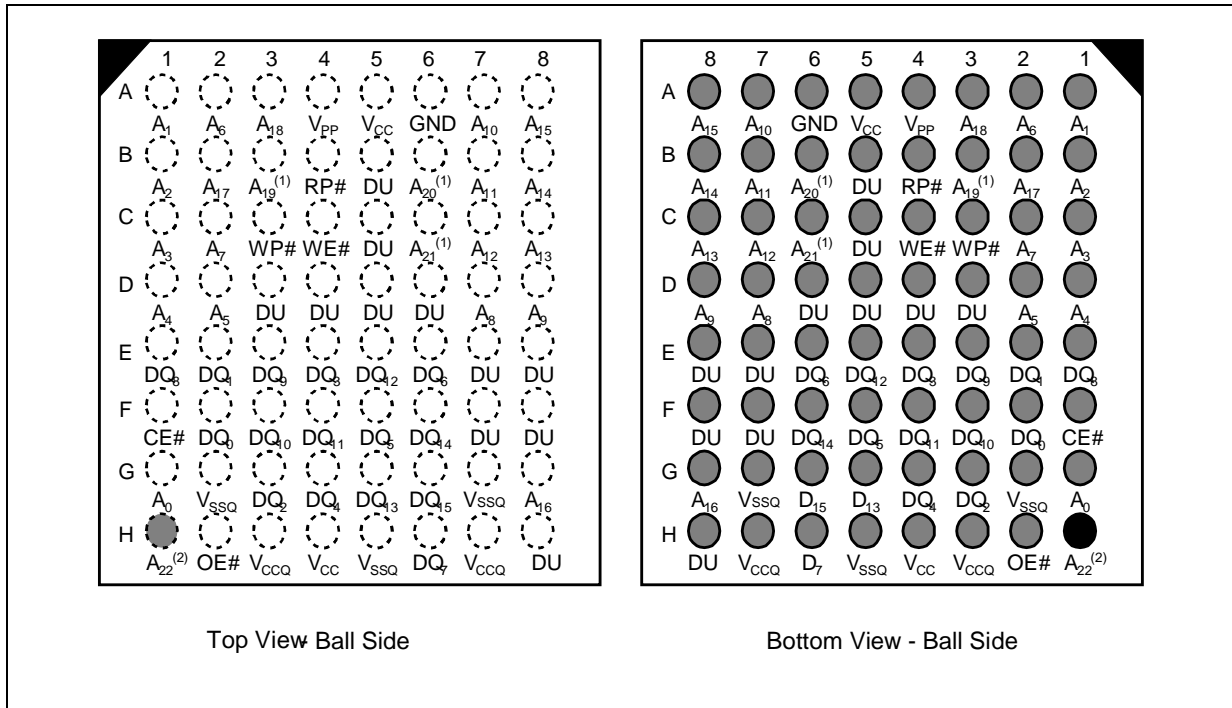
Figure 3. 48-Ball μ BGA* and 48-Ball Very Fine Pitch BGA Chip Size Package (Top View, Ball Down)



Shaded connections indicate the upgrade address connections. Lower density devices will not have the upper address solder balls. Routing is not recommended in this area. A₁₉ is the upgrade address for the 16-Mbit device. A₂₀ is the upgrade address for the 32-Mbit device. A₂₁ is the upgrade address for the 64-Mbit device.

4. 8-Mbit not available on μ BGA* CSP.

Figure 4. 8 x 8 Easy BGA Package



NOTES:

1. A₁₉ denotes 16 Mbit; A₂₀ denotes 32 Mbit; A₂₁ denotes 64 Mbit.
2. A₂₂ indicates future density upgrade path to 128 Mbit (not yet available).

16fast

Table 2. 3-Volt Advanced+ Boot Block Pin Descriptions

| Symbol | Type | Name and Function |
|-----------------------------------|------------------|--|
| A ₀ –A ₂₁ | INPUT | ADDRESS INPUTS: Memory addresses are internally latched during a program or erase cycle. 8-Mbit: A[0-18], 16-Mbit: A[0-19], 32-Mbit: A[0-20], 64-Mbit: A[0-21] |
| DQ ₀ –DQ ₇ | INPUT/ OUTPUT | DATA INPUTS/OUTPUTS: Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched. Outputs array, configuration and status register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled. |
| DQ ₈ –DQ ₁₅ | INPUT/ OUTPUT | DATA INPUTS/OUTPUTS: Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched. Outputs array and configuration data. The data pins float to tri-state when the chip is de-selected. |
| CE# | INPUT | CHIP ENABLE: Activates the internal control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels. |
| OE# | INPUT | OUTPUT ENABLE: Enables the device's outputs through the data buffers during a Read operation. OE# is active low. |
| WE# | INPUT | WRITE ENABLE: Controls writes to the command register and memory array. WE# is active low. Addresses and data are latched on the rising edge of the second WE# pulse. |
| RP# | INPUT | RESET/DEEP POWER-DOWN: Uses two voltage levels (V_{IL} , V_{IH}) to control reset/deep power-down mode. When RP# is at logic low, the device is in reset/deep power-down mode , which drives the outputs to High-Z, resets the Write State Machine, and minimizes current levels (I_{CCD}). When RP# is at logic high, the device is in standard operation. When RP# transitions from logic-low to logic-high, the device resets all blocks to locked and defaults to the read array mode. |
| WP# | INPUT | WRITE PROTECT: Controls the lock-down function of the flexible locking feature. When WP# is a logic low, the lock-down mechanism is enabled and blocks marked lock-down cannot be unlocked through software. When WP# is logic high, the lock-down mechanism is disabled and blocks previously locked-down are now locked and can be unlocked and locked through software. After WP# goes low, any blocks previously marked lock-down revert to that state. See Section 3.3 for details on block locking. |
| V _{CC} | SUPPLY | DEVICE POWER SUPPLY: [2.7 V–3.6 V] Supplies power for device operations. |
| V _{CCQ} | INPUT | I/O POWER SUPPLY: Enables all outputs to be driven to 1.8 V – 2.5 V while the V _{CC} is at 2.7 V–3.3 V. If the V _{CC} is regulated to 2.7 V–2.85 V, V _{CCQ} can be driven at 1.65 V–2.5 V to achieve lowest power operation (see Section 4.4). This input may be tied directly to V _{CC} (2.7 V–3.6 V). |
| V _{PP} | INPUT/ SUPPLY | PROGRAM/ERASE POWER SUPPLY: [1.65 V–3.6 V or 11.4 V–12.6 V] Operates as a input at logic levels to control complete device protection. Supplies power for accelerated Program and Erase operations in 12 V ± 5% range. This pin cannot be left floating. Lower V_{PP} ≤ V_{PPLK}, to protect all contents against Program and Erase commands. Set V_{PP} = V_{CC} for in-system Read, Program and Erase operations. In this configuration, V _{PP} can drop as low as 1.65 V to allow for resistor or diode drop from the system supply. Note that if V _{PP} is driven by a logic signal, V _{IH} = 1.65. That is, V _{PP} must remain above 1.65 V to perform in-system flash modifications. Raise V_{PP} to 12 V ± 5% for faster program and erase in a production environment. Applying 12 V ± 5% to V _{PP} can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V _{PP} may be connected to 12 V for a total of 80 hours maximum. See Section 3.4 for details on V _{PP} voltage configurations. |
| V _{SSQ} | SUPPLY | GROUND: For all internal circuitry. All V _{SSQ} inputs must be connected. Same function as GND. |
| GND | SUPPLY | GROUND: For all internal circuitry. All ground inputs must be connected. |
| NC | | NO CONNECT: Pin may be driven or left floating. |

2.2 Block Organization

The 3-Volt Advanced+ Boot Block is an asymmetrically blocked architecture that enables system integration of code and data within a single flash device. Each block can be erased independently of the others up to 100,000 times. For the address locations of each block, see the memory maps in [Appendix E](#).

2.2.1 Parameter Blocks

The 3-Volt Advanced+ Boot Block flash memory architecture includes parameter blocks to facilitate storage of frequently updated small parameters (i.e., data that would normally be stored in an EEPROM). Each device contains eight parameter blocks of 4 Kwords (4,096 words).

2.2.2 Main Blocks

After the parameter blocks, the remainder of the array is divided into 32-Kword (32,768 words) main blocks for data or code storage. Each 8-Mbit, 16-Mbit, 32-Mbit, or 64-Mbit device contains 15, 31, 63, or 127 main blocks, respectively.

3.0 Principles of Operation

The 3-Volt Advanced+ Boot Block flash memory family uses a CUI and automated algorithms to simplify Program and Erase operations. The CUI allows for 100% CMOS-level control inputs and fixed power supplies during erasure and programming.

The internal WSM completely automates Program and Erase operations while the CUI signals the start of an operation and the status register reports status. The CUI handles the WE# interface to the data and address latches, as well as system status requests during WSM operation.

3.1 Bus Operation

The 3-Volt Advanced+ Boot Block flash memory devices read, program, and erase in-system via the local CPU or microcontroller. All bus cycles to or from the flash memory conform to standard microcontroller bus cycles. Four control pins dictate the data flow in and out of the flash component: CE#, OE#, WE#, and RP#. [Table 3 on page 10](#) summarizes these bus operations.

3.1.1 Read

The flash memory has four read modes available: read array, read configuration, read status, and read query. These modes are accessible independent of the V_{pp} voltage. The appropriate Read Mode command must be issued to the CUI to enter the corresponding mode. Upon initial device power-up or after exit from reset, the device automatically defaults to read-array mode.

CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control; when active it enables the flash memory device. OE# is the data output control, and it drives the selected memory data onto the I/O bus. For all read modes, WE# and RP# must be at V_{IH} . [Figure 9, “AC Waveform: Read Operations” on page 35](#) illustrates a read cycle.

3.1.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins are placed in a high-impedance state.

3.1.3 Standby

Deselecting the device by bringing CE# to a logic-high level (V_{IH}) places the device in standby mode, which substantially reduces device power consumption without any latency for subsequent read accesses. In standby, outputs are placed in a high-impedance state independent of OE#. If deselected during Program or Erase operation, the device continues to consume active power until the Program or Erase operation is complete.

Table 3. Bus Operations

| Mode | Notes | RP# | CE# | OE# | WE# | DQ ₀₋₇ | DQ ₈₋₁₅ |
|---|---------|----------|----------|----------|----------|-------------------|--------------------|
| Read (Array, Status, Configuration, or Query) | 1, 2,3 | V_{IH} | V_{IL} | V_{IL} | V_{IH} | D _{OUT} | D _{OUT} |
| Output Disable | 1 | V_{IH} | V_{IL} | V_{IH} | V_{IH} | High Z | High Z |
| Standby | 1 | V_{IH} | V_{IH} | X | X | High Z | High Z |
| Reset | 1,4 | V_{IL} | X | X | X | High Z | High Z |
| Write | 1,4,5,6 | V_{IH} | V_{IL} | V_{IH} | V_{IL} | D _{IN} | D _{IN} |

NOTES:

1. X must be V_{IL} , V_{IH} for control pins and addresses.
2. See *DC Characteristics* for V_{PPLK} , V_{PP1} , V_{PP2} , V_{PP3} , voltages.
3. Manufacturer and device codes may also be accessed in read-configuration mode ($A_1-A_{20} = 0$). See [Table 4 on page 12](#).
4. To program or erase the lockable blocks, hold WP# at V_{IH} .
5. Refer to [Table 5 on page 15](#) for valid D_{IN} during a Write operation.
6. RP# must be at $GND \pm 0.2 V$ to meet the maximum deep power-down current specified.

8-bit devices use only DQ [0:7], 16-bit devices use DQ [0:15].

3.1.4 Reset

From read mode, RP# at V_{IL} for time t_{PLPH} deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. After return from reset, a time t_{PHQV} is required until the initial read-access outputs are valid. A delay (t_{PHWL} or t_{PHEL}) is required after return from reset before a write can be initiated. After this wake-up interval, normal operation is restored. The CUI resets to read-array mode, the status register is set to 80H, and all blocks are locked. [Figure 11, “AC Waveform: Reset Operations” on page 42](#) (section A) illustrates this case.

If RP# is taken low for time t_{PLPH} during a Program or Erase operation, the operation will be aborted and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, since the data may be partially erased or written. The abort process goes through the following sequence:

1. When RP# goes low, the device shuts down the operation in progress, a process which takes time t_{PLRH} to complete.
2. After this time t_{PLRH} , the part will either reset to read-array mode (if RP# has gone high during t_{PLRH} , [Figure 11](#), section B) or enter reset mode (if RP# is still logic low after t_{PLRH} , [Figure 11](#), section C).

3. In both cases, after returning from an aborted operation, the relevant time t_{PHQV} or t_{PHWL}/t_{PHEL} must be observed before a Read or Write operation is initiated, as discussed in the previous paragraph. However, in this case, these delays are referenced to the end of t_{PLRH} rather than when $RP\#$ goes high.

As with any automated device, it is important to assert $RP\#$ during system reset. When the system comes out of reset, the processor expects to read from the flash memory. Automated flash memories provide status information when read during program or Block-Erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel® Flash memories allow proper CPU initialization following a system reset through the use of the $RP\#$ input. In this application, $RP\#$ is controlled by the same $RESET\#$ signal that resets the system CPU.

3.1.5 Write

A write occurs when both $CE\#$ and $WE\#$ are low and $OE\#$ is high. Commands are written to the Command User Interface (CUI) using standard microprocessor write timings to control Flash operations. The CUI does not occupy an addressable memory location. The address and data buses are latched on the rising edge of the second $WE\#$ or $CE\#$ pulse, whichever occurs first. See [Figure 10, “AC Waveform: Program and Erase Operations” on page 41](#). The available commands are shown in [Table 6 on page 16](#), and [Appendix A](#) provides detailed information on moving between the different modes of operation using CUI commands.

Two commands modify array data: Program (40H), and Erase (20H). Writing either of these commands to the internal Command User Interface (CUI) initiates a sequence of internally timed functions that culminate in the completion of the requested task (unless that operation is aborted by either $RP\#$ being driven to V_{IL} for t_{PLRH} or an appropriate Suspend command).

3.2 Modes of Operation

The flash memory has four read modes (read array, read configuration, read status, and read query), and two write modes (program and erase). Three additional modes (erase suspend to program, erase suspend to read, and program suspend to read) are available only during suspended operations. Tables 5 and 6 summarize the commands used to reach these modes. [Appendix A](#) is a comprehensive chart showing the state transitions.

3.2.1 Read Array

When $RP\#$ transitions from V_{IL} (reset) to V_{IH} , the device defaults to read-array mode and will respond to the read-control inputs ($CE\#$, address inputs, and $OE\#$) without any additional CUI commands.

When the device is in read array mode, four control signals control data output.

- $WE\#$ must be logic high (V_{IH})
- $CE\#$ must be logic low (V_{IL})
- $OE\#$ must be logic low (V_{IL})
- $RP\#$ must be logic high (V_{IH})

In addition, the address of the desired location must be applied to the address pins. If the device is not in read-array mode, as would be the case after a Program or Erase operation, the Read Array command (FFH) must be written to the CUI before array reads can occur.

3.2.2 Read Configuration

The read-configuration mode outputs three types of information: the manufacturer/device identifier, the block locking status, and the protection register. The device is switched to this mode by writing the Read Configuration command (90H). Once in this mode, read cycles from addresses shown in Table 4 retrieve the specified information. To return to read-array mode, write the Read Array command (FFH).

Table 4. Read Configuration Table

| Item | Address | Data |
|---|----------------------|---------------------|
| Manufacturer Code (x16) | 00000 | 0089 |
| Device ID (See Appendix F) | 00001 | ID |
| Block Lock Configuration ⁽¹⁾ | XX002 ⁽²⁾ | LOCK |
| • Block Is Unlocked | | DQ ₀ = 0 |
| • Block Is Locked | | DQ ₀ = 1 |
| • Block Is Locked-Down | | DQ ₁ = 1 |
| Protection Register Lock ⁽³⁾ | 80 | PR-LK |
| Protection Register (x16) | 81–88 | PR |

NOTES:

1. See [Section 3.3.4](#) for valid lock-status outputs.
2. "XX" specifies the block address of lock configuration being read.
3. See [Section 3.4](#) for protection register information.
4. Other locations within the configuration address space are reserved by Intel for future use.

3.2.3 Read Status Register

The status register indicates the status of device operations, and the success/failure of that operation. The Read Status Register (70H) command causes subsequent reads to output data from the status register until another command is issued. To return to reading from the array, issue a Read Array (FFH) command.

The status-register bits are output on DQ₀–DQ₇. The upper byte, DQ₈–DQ₁₅, outputs 00H during a Read Status Register command.

The contents of the status register are latched on the falling edge of OE# or CE# (whichever occurs last), which prevents possible bus errors that might occur if status register contents change while being read. CE# or OE# must be toggled with each subsequent status read, or the status register will not indicate completion of a Program or Erase operation.

When the WSM is active, SR.7 will indicate the status of the WSM; the remaining bits in the status register indicate whether the WSM was successful in performing the preferred operation (see [Table 7, "Status Register Bit Definition" on page 17](#)).

3.2.3.1 Clearing the Status Register

The WSM sets status bits 1 through 7 to “1,” and clears bits 2, 6, and 7 to “0,” but cannot clear status bits 1 or 3 through 5 to “0.” Because bits 1, 3, 4, and 5 indicate various error conditions, these bits can be cleared only through the Clear Status Register (50H) command. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several addresses or erasing multiple blocks in sequence) before reading the status register to determine if an error occurred during that series. Clear the status register before beginning another command or sequence. Note that this is different from a burst device. The Read Array command must be issued before data can be read from the memory array. Resetting the device also clears the status register.

3.2.4 Read Query

The read-query mode outputs Common Flash Interface (CFI) data when the device is read, and can be accessed by writing the Read Query Command (98H). The CFI data structure contains information such as block size, density, command set, and electrical specifications. Once in this mode, read cycles from addresses shown in [Appendix C](#) retrieve the specified information. To return to read-array mode, write the Read Array command (FFH).

3.2.5 Program Mode

Programming is executed using a two-write sequence. The Program Setup command (40H) is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM will execute a sequence of internally timed events to program preferred bits of the addressed location, then verify the bits are sufficiently programmed. Programming the memory results in specific bits within an address location being changed to a “0.” If users attempt to program “1”s, the memory cell contents do not change and no error occurs.

The status register indicates programming status: while the program sequence executes, status bit 7 is “0.” The status register can be polled by toggling either CE# or OE#. While programming, the only valid commands are Read Status Register, Program Suspend, and Program Resume.

When programming is complete, the program-status bits should be checked. If the programming operation was unsuccessful, bit SR.4 of the status register is set to indicate a program failure. If SR.3 is set, then V_{PP} was not within acceptable limits, and the WSM did not execute the program command. If SR.1 is set, a program operation was attempted on a locked block and the operation was aborted.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, to prevent inadvertent status-register reads, be sure to reset the CUI to read-array mode.

3.2.5.1 Suspending and Resuming Program

The Program Suspend command halts an in-progress program operation so that data can be read from other locations of memory. Once the programming process starts, writing the Program Suspend command to the CUI requests that the WSM suspend the program sequence (at predetermined points in the program algorithm). The device continues to output status-register data after the Program Suspend command is written. Polling status-register bits SR.7 and SR.2 will determine when the program operation has been suspended (both will be set to “1”). t_{WHRH1} / t_{EHRH1} specify the program-suspend latency.

A Read Array command can now be written to the CUI to read data from blocks other than that which is suspended. The only other valid commands while program is suspended are Read Status Register, Read Configuration, Read Query, and Program Resume. After the Program Resume command is written to the flash memory, the WSM will continue with the programming process and status register bits SR.2 and SR.7 will automatically be cleared. The device automatically outputs status register data when read (see [Figure 13, “Program Suspend/Resume Flowchart” on page 49](#)) after the Program Resume command is written. V_{PP} must remain at the same V_{PP} level used for program while in program-suspend mode. $RP\#$ must also remain at V_{IH} .

3.2.6 Erase Mode

To erase a block, write the Erase Set-up and Erase Confirm commands to the CUI, along with an address identifying the block to be erased. This address is latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to “1.” Only one block can be erased at a time. The WSM will execute a sequence of internally timed events to program all bits within the block to “0,” erase all bits within the block to “1,” then verify that all bits within the block are sufficiently erased. While the erase executes, status bit 7 is a “0.”

When the status register indicates that erasure is complete, check the erase-status bit to verify that the Erase operation was successful. If the Erase operation was unsuccessful, SR.5 of the status register will be set to a “1,” indicating an erase failure. If V_{PP} was not within acceptable limits after the Erase Confirm command was issued, the WSM will not execute the erase sequence; instead, SR.5 of the status register is set to indicate an erase error, and SR.3 is set to a “1” to identify that V_{PP} supply voltage was not within acceptable limits.

After an Erase operation, clear the status register (50H) before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, to prevent inadvertent status-register reads, it is advisable to place the flash in read-array mode after the erase is complete.

3.2.6.1 Suspending and Resuming Erase

Since an Erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from—or program data to—another block in memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI suspends the erase sequence at a predetermined point in the erase algorithm. The status register will indicate if/when the Erase operation has been suspended. Erase-suspend latency is specified by t_{WHRH2}/t_{EHRH2} .

A Read Array/Program command can now be written to the CUI to read/program data from/to blocks other than that which is suspended. This nested Program command can subsequently be suspended to read yet another location. The only valid commands while Erase is suspended are Read Status Register, Read Configuration, Read Query, Program Setup, Program Resume, Erase Resume, Lock Block, Unlock Block, and Lock-Down Block. During erase-suspend mode, the chip can be placed in a pseudo-standby mode by taking $CE\#$ to V_{IH} , which reduces active current consumption.

Erase Resume continues the erase sequence when $CE\# = V_{IL}$. Similar to the end of a standard Erase operation, the status register must be read and cleared before the next instruction is issued.

Table 5. Command Bus Operations

| Command | Notes | First Bus Cycle | | | Second Bus Cycle | | |
|-----------------------|-------|-----------------|------|---------|------------------|------|------|
| | | Oper | Addr | Data | Oper | Addr | Data |
| Read Array | 1 | Write | X | FFH | | | |
| Read Configuration | 1, 2 | Write | X | 90H | Read | IA | ID |
| Read Query | 1, 2 | Write | X | 98H | Read | QA | QD |
| Read Status Register | 1 | Write | X | 70H | Read | X | SRD |
| Clear Status Register | 1 | Write | X | 50H | | | |
| Program | 1, 3 | Write | X | 40H/10H | Write | PA | PD |
| Block Erase/Confirm | 1 | Write | X | 20H | Write | BA | D0H |
| Program/Erase Suspend | 1 | Write | X | B0H | | | |
| Program/Erase Resume | 1 | Write | X | D0H | | | |
| Lock Block | 1 | Write | X | 60H | Write | BA | 01H |
| Unlock Block | 1 | Write | X | 60H | Write | BA | D0H |
| Lock-Down Block | 1 | Write | X | 60H | Write | BA | 2FH |
| Protection Program | 1 | Write | X | C0H | Write | PA | PD |

X = Don't Care PA = Prog Addr BA = Block Addr IA = Identifier Addr. QA = Query Addr.
 SRD = Status Reg. Data PD = Prog Data ID = Identifier Data QD = Query Data

NOTES:

1. Following the Read Configuration or Read Query commands, Read operations output device configuration or CFI query information, respectively. See [Section 3.2.2](#) and [Section 3.2.4](#).
2. Either 40H or 10H command is valid, but the Intel standard is 40H.
3. When writing commands, the upper data bus [DQ₈-DQ₁₅] should be either V_{IL} or V_{IH}, to minimize current draw.

Bus operations are defined in [Table 3, "Bus Operations"](#) on page 10.

Table 6. Command Codes and Descriptions

| Code | Device Mode | Description |
|------|--------------------------|--|
| FF | Read Array | This command places the device in read-array mode, which outputs array data on the data pins. |
| 40 | Program Set-Up | This is a two-cycle command. The first cycle prepares the CUI for a program operation. The second cycle latches addresses and data information and initiates the WSM to execute the Program algorithm. The flash outputs status-register data when CE# or OE# is toggled. A Read Array command is required after programming to read array data. See Section 3.2.5 . |
| 20 | Erase Set-Up | Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will (a) set both SR.4 and SR.5 of the status register to a "1," (b) place the device into the read-status-register mode, and (c) wait for another command. See Section 3.2.6 . |
| D0 | Erase Confirm | If the previous command was an Erase Set-Up command, then the CUI will close the address and data latches and begin erasing the block indicated on the address pins. During program/erase, the device will respond only to the Read Status Register, Program Suspend and Erase Suspend commands, and will output status-register data when CE# or OE# is toggled. |
| | Program/Eraser Resume | If a Program or Erase operation was previously suspended, this command will resume that operation. |
| | Unlock Block | If the previous command was Configuration Set-Up, the CUI will latch the address and unlock the block indicated on the address pins. If the block had been previously set to Lock-Down, this operation will have no effect. (Section 3.3) |
| B0 | Program Suspend | Issuing this command will begin to suspend the currently executing Program/Eraser operation. The status register will indicate when the operation has been successfully suspended by setting either the program-suspend (SR.2) or erase-suspend (SR.6) and the WSM status bit (SR.7) to a "1" (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input-control pins except RP#, which will immediately shut down the WSM and the remainder of the chip if RP# is driven to V _{IL} . See Sections 3.2.5.1 and 3.2.6.1 . |
| | Erase Suspend | |
| 70 | Read Status Register | This command places the device into read-status-register mode. Reading the device will output the contents of the status register, regardless of the address presented to the device. The device automatically enters this mode after a Program or Erase operation has been initiated. See Section 3.2.3 . |
| 50 | Clear Status Register | The WSM can set the block-lock status (SR.1), V _{PP} Status (SR.3), program status (SR.4), and erase-status (SR.5) bits in the status register to "1," but it cannot clear them to "0." Issuing this command clears those bits to "0." |
| 90 | Read Configuration | Puts the device into the read-configuration mode so that reading the device will output the manufacturer/device codes or block-lock status. Section 3.2.2 . |
| 60 | Configuration Set-Up | Prepares the CUI for changes to the device configuration, such as block-locking changes. If the next command is not Block Unlock, Block Lock, or Block Lock-Down, then the CUI will set both the program and erase-status-register bits to indicate a command-sequence error. See Section 3.2 . |
| 01 | Lock-Block | If the previous command was Configuration Set-Up, the CUI will latch the address and lock the block indicated on the address pins. (Section 3.3) |
| 2F | Lock-Down | If the previous command was a Configuration Set-Up command, the CUI will latch the address and lock-down the block indicated on the address pins. (Section 3.3) |
| 98 | Read Query | Puts the device into the read-query mode so that reading the device will output Common Flash Interface information. See Section 3.2.4 and Appendix C . |
| C0 | Protection Program Setup | This is a two-cycle command. The first cycle prepares the CUI for a program operation to the protection register. The second cycle latches addresses and data information and initiates the WSM to execute the Protection Program algorithm to the protection register. The flash outputs status-register data when CE# or OE# is toggled. A Read Array command is required after programming to read array data. See Section 3.4 . |
| 10 | Alt. Prog Set-Up | Operates the same as Program Set-up command. (See 40H/Program Set-Up) |
| 00 | Invalid/Reserved | Unassigned commands that should not be used. Intel reserves the right to redefine these codes for future functions. |

NOTE: See [Appendix A](#) for mode transition information.

Table 7. Status Register Bit Definition

| WSMS | ESS | ES | PS | VPPS | PSS | BLS | R |
|---|-----|----|----|---|-----|-----|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | NOTES: | | | |
| SR.7 WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy | | | | Check Write State Machine bit first to determine Word Program or Block Erase completion, before checking program or erase-status bits. | | | |
| SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed | | | | When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an Erase Resume command is issued. | | | |
| SR.5 = ERASE STATUS (ES) 1 = Error In Block Erase 0 = Successful Block Erase | | | | When this bit is set to "1," WSM has applied the max. number of erase pulses to the block and is still unable to verify successful block erasure. | | | |
| SR.4 = PROGRAM STATUS (PS) 1 = Error in Programming 0 = Successful Programming | | | | When this bit is set to "1," WSM has attempted but failed to program a word/byte. | | | |
| SR.3 = V _{PP} STATUS (VPPS) 1 = V _{PP} Low Detect, Operation Abort 0 = V _{PP} OK | | | | The V _{PP} status bit does not provide continuous indication of V _{PP} level. The WSM interrogates V _{PP} level only after the Program or Erase command sequences have been entered, and informs the system if V _{PP} has not been switched on. The V _{PP} is also checked before the operation is verified by the WSM. The V _{PP} status bit is not guaranteed to report accurate feedback between V _{PPLK} and V _{PP1Min} . | | | |
| SR.2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed | | | | When Program Suspend is issued, WSM halts execution and sets both WSMS and PSS bits to "1." PSS bit remains set to "1" until a Program Resume command is issued. | | | |
| SR.1 = BLOCK LOCK STATUS 1 = Prog/Erase attempted on a locked block; Operation aborted. 0 = No operation to locked blocks | | | | If a Program or Erase operation is attempted to one of the locked blocks, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode. | | | |
| SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R) | | | | This bit is reserved for future use and should be masked out when polling the status register. | | | |

NOTE: A Command-Sequence Error is indicated when SR.4, SR.5, and SR.7 are set.

3.3 Flexible Block Locking

Intel 3-Volt Advanced+ Boot Block products offer an instant, individual block-locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection.

This locking scheme offers two levels of protection. The first level allows software-only control of block locking (useful for data blocks that change frequently), while the second level requires hardware interaction before locking can be changed (useful for code blocks that change infrequently).

The following sections will discuss the operation of the locking system. The term "state [XYZ]" will be used to specify locking states; e.g., "state [001]," where X = value of WP#, Y = bit DQ₁ of the Block Lock status register, and Z = bit DQ₀ of the Block Lock status register. [Table 9, "Block Locking State Transitions" on page 20](#) defines all of these possible locking states.

3.3.1 Locking Operation

The following concisely summarizes the locking functionality.

- All blocks power-up locked, then can be unlocked or locked with the Unlock and Lock commands.
- The Lock-Down command locks a block and prevents it from being unlocked when WP# = 0.
 - When WP# = 1, Lock-Down is overridden and commands can unlock/lock locked-down blocks.
 - When WP# returns to 0, locked-down blocks return to Lock Down.
 - Lock Down is cleared only when the device is reset or powered down.

The locking status of each block can be set to Locked, Unlocked, and Lock Down, each of which will be described in the following sections. [Table 9 on page 20](#) is a comprehensive state table for the locking functions; [Figure 16 on page 52](#) is a flowchart for Locking operations.

3.3.1.1 Locked State

The default status of all blocks upon power-up or reset is locked (states [001] or [101]). Locked blocks are fully protected from alteration. Any Program or Erase operations attempted on a locked block will return an error on bit SR.1 of the status register. The status of a locked block can be changed to Unlocked or Lock Down using the appropriate software commands. An Unlocked block can be locked by writing the Lock command sequence, 60H followed by 01H.

3.3.2 Unlocked State

Unlocked blocks (states [000], [100], [110]) can be programmed or erased. All unlocked blocks return to the Locked state when the device is reset or powered down. The status of an unlocked block can be changed to Locked or Locked Down using the appropriate software commands. A Locked block can be unlocked by writing the Unlock command sequence, 60H followed by D0H.

3.3.3 Lock-Down State

Blocks that are Locked Down (state [011]) are protected from Program and Erase operations (just like Locked blocks), but their protection status cannot be changed using software commands alone. A Locked or Unlocked block can be Locked Down by writing the Lock-Down command sequence, 60H followed by 2FH. Locked-Down blocks revert to the Locked state when the device is reset or powered down.

The Lock-Down function depends on the WP# input pin. When WP# = 0, blocks in Lock Down [011] are protected from program, erase, and lock status changes. When WP# = 1, the Lock-Down function is disabled ([111]) and Locked-Down blocks can be individually unlocked by software command to the [110] state, where they can be erased and programmed. These blocks can then be relocked [111] and unlocked [110] as required while WP# remains high. When WP# goes low, blocks that were previously Locked Down return to the Lock-Down state [011], regardless of any changes made while WP# was high. Device reset or power-down resets all blocks, including those in Lock-Down, to Locked state.

3.3.4 Reading Block-Lock Status

The Lock status of every block can be read in the configuration-read mode of the device. To enter this mode, write 90H to the device. Subsequent reads at Block Address + 00002 will output the Lock status of that block. The Lock status is represented by DQ₀ and DQ₁. DQ₀ indicates the Block Lock/Unlock status and is set by the Lock command and cleared by the Unlock command. It is also automatically set when entering Lock Down. DQ₁ indicates Lock-Down status, and is set by the Lock-Down command. It cannot be cleared by software—only by device reset or power-down.

Table 8. Block Lock Status

| Item | Address | Data |
|--------------------------|---------|---------------------|
| Block Lock Configuration | XX002 | LOCK |
| • Block Is Unlocked | | DQ ₀ = 0 |
| • Block Is Locked | | DQ ₀ = 1 |
| • Block Is Locked-Down | | DQ ₁ = 1 |

3.3.5 Locking Operations during Erase Suspend

Changes to block-lock status can be performed during an erase-suspend by using the standard locking command sequences to Unlock, Lock, or Lock Down a block. This is useful in the case when another block needs to be updated while an Erase operation is in progress.

To change block locking during an Erase operation, first write the Erase Suspend command (B0H), then check the status register until it indicates that the Erase operation has been suspended. Next, write the preferred Lock command sequence to a block and the Lock status will be changed. After completing any preferred Lock, Read, or Program operations, resume the Erase operation with the Erase Resume command (D0H).

If a block is Locked or Locked Down during a Suspended Erase of the same block, the locking status bits will be changed immediately, but when the Erase is resumed, the Erase operation will complete.

Locking operations cannot be performed during a Program Suspend. Refer to [Appendix A](#) for detailed information on which commands are valid during Erase Suspend.

3.3.6 Status Register Error Checking

Using nested-locking or program-command sequences during Erase Suspend can introduce ambiguity into status register results.

Since locking changes are performed using a two-cycle command sequence, e.g., 60H followed by 01H to lock a block, following the Configuration Setup command (60H) with an invalid command will produce a Lock-Command error (SR.4 and SR.5 will be set to 1) in the status register. If a Lock-Command error occurs during an Erase Suspend, SR.4 and SR.5 will be set to 1 and will remain at 1 after the Erase is resumed. When Erase is complete, any possible error during the Erase cannot be detected via the status register because of the previous Lock-Command error.

A similar situation happens if an error occurs during a Program-Operation error nested within an Erase Suspend.

Table 9. Block Locking State Transitions

| Current State | | | | Erase/Prog Allowed? | Lock Command Input Result (Next State) | | |
|---------------|-----------------|-----------------|--------------------|------------------------|--|---------------|---------------|
| X | Y | Z | | | Lock | Unlock | Lock-Down |
| WP# | DQ ₁ | DQ ₀ | Name | | | | |
| 0 | 0 | 0 | "Unlocked" | Yes | Goes To [001] | No Change | Goes To [011] |
| 0 | 0 | 1 | "Locked" (Default) | No | No Change | Goes To [000] | Goes To [011] |
| 0 | 1 | 1 | "Locked-Down" | No | No Change | No Change | No Change |
| 1 | 0 | 0 | "Unlocked" | Yes | Goes To [101] | No Change | Goes To [111] |
| 1 | 0 | 1 | "Locked" | No | No Change | Goes To [100] | Goes To [111] |
| 1 | 1 | 0 | Lock-Down Disabled | Yes | Goes To [111] | No Change | Goes To [111] |
| 1 | 1 | 1 | Lock-Down Disabled | No | No Change | Goes To [110] | No Change |

NOTES:

- In this table, the notation [XYZ] denotes the locking state of a block, where X = WP#, Y = DQ₁, and Z = DQ₀. The current locking state of a block is defined by the state of WP# and the two bits of the block-lock status (DQ₀, DQ₁). DQ₀ indicates if a block is locked (1) or unlocked (0). DQ₁ indicates if a block has been Locked Down (1) or not (0).
- At power-up or device reset, all blocks default to Locked state [001] (if WP# = 0). Holding WP# = 0 is the recommended default.
- The "Erase/Program Allowed?" column shows whether Erase and Program operations are enabled (Yes) or disabled (No) in that block's current Lock state.
- The "Lock Command Input Result [Next State]" column shows the result of writing the three Lock commands (Lock, Unlock, Lock-Down) in the current Lock state. For example, "Goes To [001]" would mean that writing the command to a block in the current Lock state would change it to [001].

3.4 128-Bit Protection Register

The 3-Volt Advanced+ Boot Block architecture includes a 128-bit protection register that can be used to increase the security of a system design. For example, the number contained in the protection register can be used to "mate" the flash component with other system components, such as the CPU or ASIC, preventing device substitution. The Intel application note, *AP-657 Designing with the Advanced+ Boot Block Flash Memory Architecture*, contains additional application information.

The 128 bits of the protection register are divided into two 64-bit segments. One of the segments is programmed at the Intel factory with a unique 64-bit number, which is unchangeable. The other segment is left blank for customer designs to program, as preferred. Once the customer segment is programmed, it can be locked to prevent reprogramming.

3.4.1 Reading the Protection Register

The protection register is read in the configuration-read mode. The device is switched to this mode by writing the Read Configuration command (90H). Once in this mode, read cycles from addresses shown in [Appendix G](#) retrieve the specified information. To return to read-array mode, write the Read Array command (FFH).

3.4.2 Programming the Protection Register

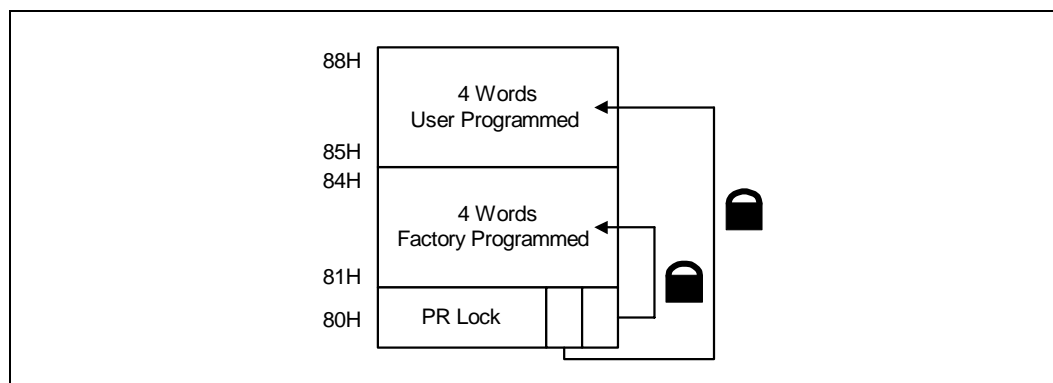
The protection register bits are programmed using the two-cycle Protection Program command. The 64-bit number is programmed 16 bits at a time for word-wide parts, and eight bits at a time for byte-wide parts.

First, write the Protection Program Setup command, C0H. The next write to the device will latch in address and data, and program the specified location. The allowable addresses are shown in Appendix G. See Figure 17, “Protection Register Programming Flowchart” on page 53. Attempts to address Protection Program commands outside the defined protection register address space should not be attempted. This space is reserved for future use. Attempting to program to a previously locked protection register segment will result in a Status Register error (Program Error bit SR.4 and Lock Error bit SR.1 will be set to 1).

3.4.3 Locking the Protection Register

The user-programmable segment of the protection register is lockable by programming Bit 1 of the PR-LOCK location to 0. Bit 0 of this location is programmed to 0 at the Intel factory to protect the unique device number. This bit is set using the Protection Program command to program “FFFD” to the PR-LOCK location. After these bits have been programmed, no further changes can be made to the values stored in the protection register. Protection Program commands to a locked section will result in a Status Register error (Program Error bit SR.4 and Lock Error bit SR.1 will be set to 1). Protection register lockout state is not reversible.

Figure 5. Protection Register Memory Map



0645_05

3.5 V_{PP} Program and Erase Voltages

Intel 3-Volt Advanced+ Boot Block products provide in-system programming and erase in the 1.65 V–3.6 V range. For fast production programming, it also includes a low-cost, backward-compatible 12-V programming feature.

3.5.1 Improved 12-Volt Production Programming

When V_{PP} is between 1.65 V and 3.6 V, all program and erase current is drawn through the V_{CC} pin. Note that if V_{PP} is driven by a logic signal, V_{IH} min = 1.65 V. That is, V_{PP} must remain above 1.65 V to perform in-system flash modifications. When V_{PP} is connected to a 12 V power supply,

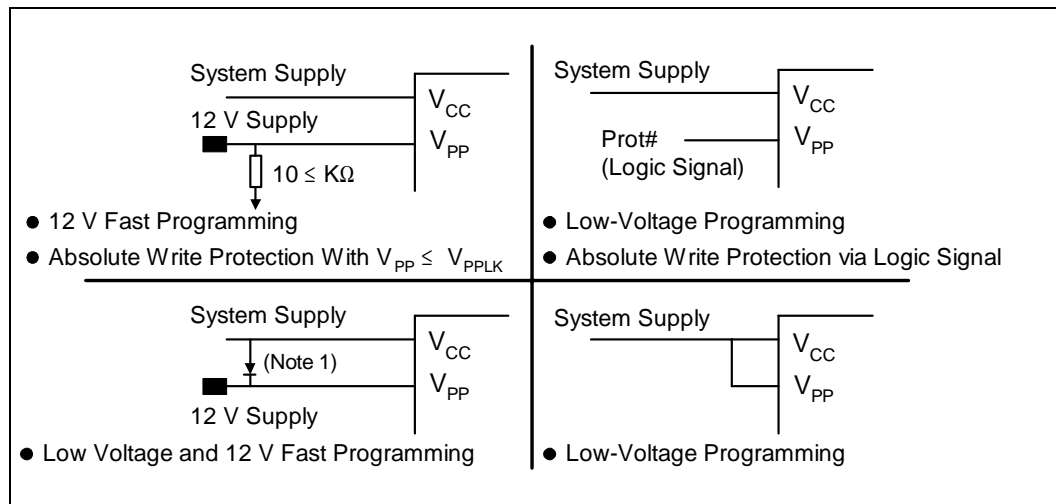
the device draws program and erase current directly from the V_{PP} pin. This eliminates the need for an external switching transistor to control the voltage V_{PP} . Figure 6 on page 22 shows examples of how the flash power supplies can be configured for various usage models.

The 12-V V_{PP} mode enhances programming performance during the short period of time typically found in manufacturing processes; however, it is not intended for extended use. 12 V may be applied to V_{PP} during Program and Erase operations for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum. Stressing the device beyond these limits may cause permanent damage.

3.5.2 $V_{PP} \leq V_{PPLK}$ for Complete Protection

In addition to the flexible block locking, the V_{PP} programming voltage can be held low for absolute hardware write protection of all blocks in the flash device. When V_{PP} is below V_{PPLK} , any Program or Erase operation will result in an error, prompting the corresponding status-register bit (SR.3) to be set.

Figure 6. Example Power Supply Configurations



NOTE:

1. A resistor can be used if the V_{CC} supply can sink adequate current based on resistor value. See AP-657 *Designing with the Advanced+ Boot Block Flash Memory Architecture* for details.

0645_06

3.6 Power Consumption

Intel Flash devices have a tiered approach to power savings that can significantly reduce overall system power consumption. The Automatic Power Savings (APS) feature reduces power consumption when the device is selected but idle. If the $CE\#$ is deasserted, the flash enters its standby mode, where current consumption is even lower. The combination of these features can minimize memory power consumption, and therefore, overall system power consumption.

3.6.1 Active Power (Program/Erase/Read)

With CE# at a logic-low level and RP# at a logic-high level, the device is in the active mode. Refer to the DC Characteristic tables for I_{CC} current values. Active power is the largest contributor to overall system power consumption. Minimizing the active current could have a profound effect on system power consumption, especially for battery-operated devices.

3.6.2 Automatic Power Savings (APS)

Automatic Power Savings provides low-power operation during read mode. After data is read from the memory array and the address lines are quiescent, APS circuitry places the device in a mode where typical current is comparable to I_{CCS} . The flash stays in this static state with outputs valid until a new location is read.

3.6.3 Standby Power

When CE# is at a logic-high level (V_{IH}) and the device is in read mode, the flash memory is in standby mode, which disables much of the device's circuitry and substantially reduces power consumption. Outputs are placed in a high-impedance state independent of the status of the OE# signal. If CE# transitions to a logic-high level during Erase or Program operations, the device will continue to perform the operation and consume corresponding active power until the operation is completed.

System engineers should analyze the breakdown of standby time versus active time, and quantify the respective power consumption in each mode for their specific application. This approach will provide a more accurate measure of application-specific power and energy requirements.

3.6.4 Deep Power-Down Mode

The deep power-down mode is activated when $RP\# = V_{IL}$ ($GND \pm 0.2 V$). During read modes, RP# going low de-selects the memory and places the outputs in a high-impedance state. Recovery from deep power-down requires a minimum time of t_{PHQV} for Read operations, and t_{PHWL}/t_{PHEL} for Write operations.

During program or erase modes, RP# transitioning low will abort the in-progress operation. The memory contents of the address being programmed or the block being erased are no longer valid as the data integrity has been compromised by the abort. During deep power-down, all internal circuits are switched to a low-power savings mode (RP# transitioning to V_{IL} or turning off power to the device clears the status register).

3.7 Power-Up/Down Operation

The device is protected against accidental block erasure or programming during power transitions. Power supply sequencing is not required, because the device is indifferent as to which power supply, V_{PP} or V_{CC} , powers-up first.

3.7.1 RP# Connected to System Reset

The use of RP# during system reset is important with automated program/erase devices since the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization will not occur because the flash memory may be providing status information instead of array data. Intel recommends connecting RP# to the system CPU RESET# signal to allow proper CPU/flash initialization following system reset.

System designers must guard against spurious writes when V_{CC} voltages are above V_{LKO} . Because both WE# and CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until RP# is brought to V_{IH} , regardless of the state of its control inputs. By holding the device in reset (RP# connected to system POWERGOOD) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

3.7.2 V_{CC} , V_{PP} and RP# Transitions

The CUI latches commands as issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its default state upon power-up, after exit from reset mode or after V_{CC} transitions above V_{LKO} (Lockout voltage), is read-array mode.

After any program or Block-Erase operation is complete (even after V_{PP} transitions down to V_{PPLK}), the CUI must be reset to read-array mode via the Read Array command if access to the flash-memory array is desired.

3.8 Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers should consider the following three supply current issues:

- Standby current levels (I_{CCS})
- Read current levels (I_{CCR})
- Transient peaks produced by falling and rising edges of CE#.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 μ F ceramic capacitor connected between each V_{CC} and GND, and between its V_{PP} and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

| Parameter | Maximum Rating |
|--|--------------------------------------|
| Extended Operating Temperature | |
| During Read | -40 °C to +85 °C |
| During Block Erase and Program | -40 °C to +85 °C |
| Temperature under Bias | -40 °C to +85 °C |
| Storage Temperature | -65 °C to +125 °C |
| Voltage On Any Pin (except V _{CC} and V _{PP}) with Respect to GND | -0.5 V to +3.7 V ⁽¹⁾ |
| V _{PP} Voltage (for Block Erase and Program) with Respect to GND | -0.5 V to +13.5 V ^(1,2,3) |
| V _{CC} and V _{CCQ} Supply Voltage with Respect to GND | -0.2 V to +3.6 V |
| Output Short Circuit Current | 100 mA ⁽⁴⁾ |

NOTES:

1. Minimum DC voltage is -0.5 V on input/output pins. During transitions, this level may undershoot to -2.0 V for periods <20 ns. Maximum DC voltage on input/output pins is V_{CC} +0.5 V which, during transitions, may overshoot to V_{CC} +2.0 V for periods <20 ns.
2. Maximum DC voltage on V_{PP} may overshoot to +14.0 V for periods <20 ns.
3. V_{PP} Program voltage is normally 1.65 V–3.6 V. Connection to a 11.4 V–12.6 V supply can be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase. V_{PP} may be connected to 12 V for a total of 80 hours maximum. See [Section 3.5](#) for details.
4. Output shorted for no more than one second. No more than one output shorted at a time.

NOTICE: This datasheet contains preliminary information on new products in production. Specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

4.2 Operating Conditions

Table 10. Temperature and Voltage Operating Conditions

| Symbol | Parameter | Notes | Min | Max | Units |
|------------|--------------------------------|-------|---------|------|--------|
| T_A | Operating Temperature | | -40 | +85 | °C |
| V_{CC1} | V _{CC} Supply Voltage | 1, 2 | 2.7 | 3.6 | Volts |
| V_{CC2} | | 1, 2 | 3.0 | 3.6 | |
| V_{CCQ1} | I/O Supply Voltage | 1 | 2.7 | 3.6 | Volts |
| V_{CCQ2} | | | 1.65 | 2.5 | |
| V_{CCQ3} | | | 1.8 | 2.5 | |
| V_{PP1} | Supply Voltage | 1 | 1.65 | 3.6 | Volts |
| V_{PP2} | | 1, 3 | 11.4 | 12.6 | Volts |
| Cycling | Block Erase Cycling | 3 | 100,000 | | Cycles |

NOTES:

1. V_{CC} and V_{CCQ} must share the same supply when they are in the V_{CC1} range.
2. V_{CCMax} = 3.3 V for 0.25μm 32-Mbit devices.
3. Applying V_{PP} = 11.4 V–12.6 V during a program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum. See [Section 3.5](#) for details.

4.3 Capacitance

$T_A = 25\text{ °C}$, $f = 1\text{ MHz}$

| Sym | Parameter | Notes | Typ | Max | Units | Conditions |
|-----------|--------------------|-------|-----|-----|-------|------------------------|
| C_{IN} | Input Capacitance | 1 | 6 | 8 | pF | $V_{IN} = 0\text{ V}$ |
| C_{OUT} | Output Capacitance | 1 | 10 | 12 | pF | $V_{OUT} = 0\text{ V}$ |

NOTE:

1. Sampled, not 100% tested.

4.4 DC Characteristics

| Sym | Parameter | V _{CC} | 2.7 V–3.6 V | | 2.7 V–2.85 V | | 2.7 V–3.3 V | | Unit | Test Conditions |
|---------------------------------------|--|------------------|-------------|------|--------------|------|-------------|------|------|--|
| | | V _{CCQ} | 2.7 V–3.6 V | | 1.65 V–2.5 V | | 1.8 V–2.5 V | | | |
| | | Note | Typ | Max | Typ | Max | Typ | Max | | |
| I _{LI} | Input Load Current | 1,2 | | ± 1 | | ± 1 | | ± 1 | µA | V _{CC} = V _{CC} Max V _{CCQ} = V _{CCQ} Max V _{IN} = V _{CCQ} or GND |
| I _{LO} | Output Leakage Current | 1,2 | 0.2 | ± 10 | 0.2 | ± 10 | 0.2 | ± 10 | µA | V _{CC} = V _{CC} Max V _{CCQ} = V _{CCQ} Max V _{IN} = V _{CCQ} or GND |
| I _{CCS} | V _{CC} Standby Current for 0.13 and 0.18 Micron Product | 1 | 7 | 15 | 20 | 50 | 150 | 250 | µA | V _{CC} = V _{CC} Max CE# = RP# = V _{CCQ} or during Program/ Erase Suspend WP# = V _{CCQ} or GND |
| | V _{CC} Standby Current for 0.25 Micron Product | 1 | 10 | 25 | 20 | 50 | 150 | 250 | µA | |
| I _{CCD} | V _{CC} Power-Down Current for 0.13 and 0.18 Micron Product | 1,2 | 7 | 15 | 7 | 20 | 7 | 20 | µA | V _{CC} = V _{CC} Max V _{CCQ} = V _{CCQ} Max V _{IN} = V _{CCQ} or GND RP# = GND ± 0.2 V |
| | V _{CC} Power-Down Current for 0.25 Micron Product | 1,2 | 7 | 25 | 7 | 25 | 7 | 25 | µA | |
| I _{CCR} | V _{CC} Read Current for 0.13 and 0.18 Micron Product | 1,2,3 | 9 | 18 | 8 | 15 | 9 | 15 | mA | V _{CC} = V _{CC} Max V _{CCQ} = V _{CCQ} Max OE# = V _{IH} , CE# = V _{IL} f = 5 MHz, I _{OUT} = 0 mA Inputs = V _{IL} or V _{IH} |
| | V _{CC} Read Current for 0.25 Micron Product | 1,2,3 | 10 | 18 | 8 | 15 | 9 | 15 | mA | |
| I _{PPD} | V _{PP} Deep Power-Down Current | 1 | 0.2 | 5 | 0.2 | 5 | 0.2 | 5 | µA | RP# = GND ± 0.2 V V _{PP} ≤ V _{CC} |
| I _{PPR} | V _{PP} Read Current | 1,4 | 2 | ±15 | 2 | ±15 | 2 | ±15 | µA | V _{PP} ≤ V _{CC} |
| | | | 50 | 200 | 50 | 200 | 50 | 200 | µA | V _{PP} > V _{CC} |
| I _{CCW+} I _{PPW} | V _{CC} + V _{PP} Program Current for 0.13 and 0.18 Micron Product | 1,4 | 0.05 | 0.1 | 18 | 55 | 18 | 55 | mA | V _{PP} = V _{PP1} , Program in Progress |
| | | | 8 | 22 | 10 | 30 | 10 | 30 | mA | V _{PP} = V _{PP2} (12V) Program in Progress |
| | V _{CC} + V _{PP} Program Current for 0.25 Micron Product | 1,4 | 0.05 | 0.1 | 18 | 55 | 18 | 55 | mA | V _{PP} = V _{PP1} , Program in Progress |
| | | | 8 | 22 | 10 | 30 | 10 | 30 | mA | V _{PP} = V _{PP2} (12V) Program in Progress |

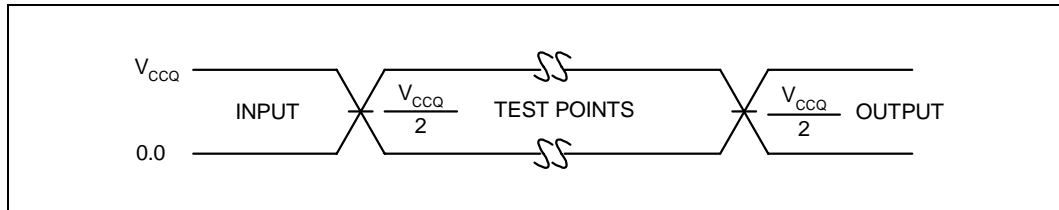
| Sym | Parameter | V _{CC} | 2.7 V–3.6 V | | 2.7 V–2.85 V | | 2.7 V–3.3 V | | Unit | Test Conditions |
|---------------------------------------|---|------------------|------------------------|--------------------------|------------------------|------------------------|------------------------|------------------------|------|---|
| | | V _{CCQ} | 2.7 V–3.6 V | | 1.65 V–2.5 V | | 1.8 V–2.5 V | | | |
| | | Note | Typ | Max | Typ | Max | Typ | Max | | |
| I _{CCCE} + I _{PPPE} | V _{CC} + V _{PP} Erase Current for 0.13 and 0.18 Micron Product | 1,4 | 0.05 | 0.1 | 21 | 45 | 21 | 45 | mA | V _{PP} = V _{PP1} , Erase in Progress |
| | | | 8 | 22 | 16 | 45 | 16 | 45 | mA | V _{PP} = V _{PP2} (12V), Erase in Progress |
| | V _{CC} + V _{PP} Erase Current for 0.25 Micron Product | 1,4 | 0.05 | 0.1 | 21 | 45 | 21 | 45 | mA | V _{PP} = V _{PP1} , Erase in Progress |
| | | | 8 | 22 | 16 | 45 | 16 | 45 | mA | V _{PP} = V _{PP2} (12V), Erase in Progress |
| I _{PPES} + I _{PPWS} | V _{CC} + V _{PP} Program or Erase Suspend Current for 0.13 and 0.18 Micron Product | 1,4 | 0.05 | 0.1 | 21 | 45 | 21 | 45 | μA | V _{PP} = V _{PP1} , Program or Erase Suspend in Progress |
| | | | 50 | 200 | 50 | 200 | 50 | 200 | μA | V _{PP} = V _{PP2} (12V), Program or Erase Suspend in Progress |
| | V _{CC} + V _{PP} Program or Erase Suspend Current for 0.25 Micron Product | 1,4 | 0.05 | 0.1 | 21 | 45 | 21 | 45 | μA | V _{PP} = V _{PP1} , Program or Erase Suspend in Progress |
| | | | 50 | 200 | 50 | 200 | 50 | 200 | μA | V _{PP} = V _{PP2} (12V), Program or Erase Suspend in Progress |
| V _{IL} | Input Low Voltage | | -0.4 | V _{CC} * 0.22 V | -0.4 | 0.4 | -0.4 | 0.4 | V | |
| V _{IH} | Input High Voltage | | 2.0 | V _{CCQ} +0.3V | V _{CCQ} -0.4V | V _{CCQ} +0.3V | V _{CCQ} -0.4V | V _{CCQ} +0.3V | V | |
| V _{OL} | Output Low Voltage | | -0.1 | 0.1 | -0.1 | 0.1 | -0.1 | 0.1 | V | V _{CC} = V _{CCMin} V _{CCQ} = V _{CCQMin} I _{OL} = 100 μA |
| V _{OH} | Output High Voltage | | V _{CCQ} -0.1V | | V _{CCQ} -0.1V | | V _{CCQ} -0.1V | | V | V _{CC} = V _{CCMin} V _{CCQ} = V _{CCQMin} I _{OH} = -100 μA |
| V _{PPLK} | V _{PP} Lock-Out Voltage | 6 | | 1.0 | | 1.0 | | 1.0 | V | Complete Write Protection |
| V _{PP1} | V _{PP} during Program / Erase Operations | 6 | 1.65 | 3.6 | | | | | V | |
| V _{PP2} | | 6, 7 | | | 11.4 | 12.6 | | | V | |
| V _{LKO} | V _{CC} Prog/Erase Lock Voltage | | 1.5 | | 1.5 | | 1.5 | | V | |
| V _{LKO2} | V _{CCQ} Prog/Erase Lock Voltage | | 1.2 | | 1.2 | | 1.2 | | V | |

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC}, T_A = +25 °C.
2. The test conditions V_{CC}Max, V_{CCQ}Max, V_{CC}Min, and V_{CCQ}Min refer to the maximum or minimum V_{CC} or V_{CCQ} voltage listed at the top of each column. V_{CC}Max = 3.3 V for 0.25μm 32-Mbit devices.
3. Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels in static operation (CMOS inputs).
4. Sampled, not 100% tested.
5. I_{CCES} and I_{CCWS} are specified with device de-selected. If device is read while in erase suspend, current draw is sum of I_{CCES} and I_{CCR}. If the device is read while in program suspend, current draw is the sum of I_{CCWS} and I_{CCR}.

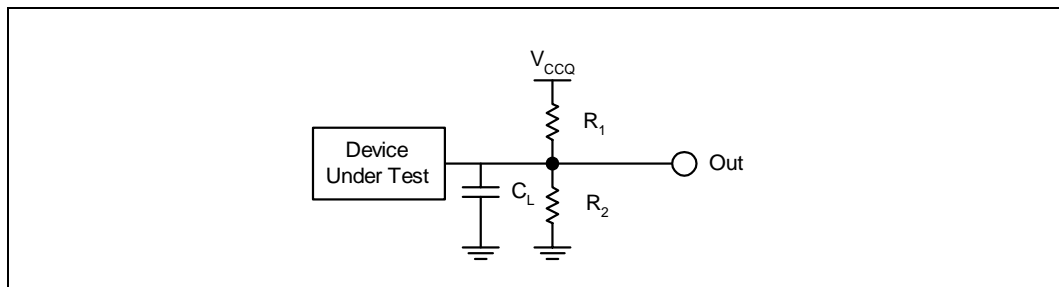
6. Erase and Program are inhibited when $V_{PP} < V_{PPLK}$ and not guaranteed outside the valid V_{PP} ranges of V_{PP1} and V_{PP2} .
7. Applying $V_{PP} = 11.4\text{ V} - 12.6\text{ V}$ during program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum. See [Section 3.4](#) for details.

Figure 7. Input/Output Reference Waveform



0645_07

Figure 8. Test Configuration



0645_08

| Test Configuration | C_L (pF) | R_1 (Ω) | R_2 (Ω) |
|---------------------------|------------|--------------------|--------------------|
| 2.7 V–3.6 V Standard Test | 50 | 25K | 25K |

NOTE: C_L includes jig capacitance.

4.5 AC Characteristics—Read Operations

| # | Sym | Parameter | Density | 8 Mbit | | | | | | | | Unit |
|-----|-------------------|--|-----------------|---------------|-----|---------------|-----|---------------|-----|---------------|-----|------|
| | | | Product | 90 ns | | | | 110 ns | | | | |
| | | | V _{CC} | 3.0 V – 3.6 V | | 2.7 V – 3.6 V | | 3.0 V – 3.6 V | | 2.7 V – 3.6 V | | |
| | | | Note | Min | Max | Min | Max | Min | Max | Min | Max | |
| R1 | t _{AVAV} | Read Cycle Time | | 80 | | 90 | | 100 | | 110 | | ns |
| R2 | t _{AVQV} | Address to Output Delay | | | 80 | | 90 | | 100 | | 110 | ns |
| R3 | t _{ELQV} | CE# to Output Delay | 1 | | 80 | | 90 | | 100 | | 110 | ns |
| R4 | t _{GLQV} | OE# to Output Delay | 1 | | 30 | | 30 | | 30 | | 30 | ns |
| R5 | t _{PHQV} | RP# to Output Delay | | | 150 | | 150 | | 150 | | 150 | ns |
| R6 | t _{ELQX} | CE# to Output in Low Z | 2 | 0 | | 0 | | 0 | | 0 | | ns |
| R7 | t _{GLQX} | OE# to Output in Low Z | 2 | 0 | | 0 | | 0 | | 0 | | ns |
| R8 | t _{EHQZ} | CE# to Output in High Z | 2 | | 20 | | 20 | | 20 | | 20 | ns |
| R9 | t _{GHQZ} | OE# to Output in High Z | 2 | | 20 | | 20 | | 20 | | 20 | ns |
| R10 | t _{OH} | Output Hold from Address, CE#, or OE# Change, Whichever Occurs First | 2 | 0 | | 0 | | 0 | | 0 | | ns |

NOTES:

1. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.

See [Figure 9, “AC Waveform: Read Operations”](#) on page 35.

See [Figure 7, “Input/Output Reference Waveform”](#) on page 30 for timing measurements and maximum allowable input slew rate.

AC Characteristics—Read Operations, continued

| # | Sym | Parameter | Density | 16 Mbit | | | | | | | | | | | | Unit |
|-----|-------------------|---|-----------------|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------------|-----|------|
| | | | Product | 70 ns | | 80 ns | | 90 ns | | | | 110 ns | | | | |
| | | | V _{CC} | 2.7 V–3.6 V | | 2.7 V–3.6 V | | 3.0 V–3.6 V | | 2.7 V–3.6 V | | 3.0 V–3.6 V | | 2.7 V–3.6 V | | |
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| R1 | t _{AVAV} | Read Cycle Time | | 70 | | 80 | | 80 | | 90 | | 100 | | 110 | | ns |
| R2 | t _{AVQV} | Address to Output Delay | | 70 | | 80 | | 80 | | 90 | | 100 | | 110 | | ns |
| R3 | t _{ELQV} | CE# to Output Delay ⁽¹⁾ | | 70 | | 80 | | 80 | | 90 | | 100 | | 110 | | ns |
| R4 | t _{GLQV} | OE# to Output Delay ⁽¹⁾ | | 20 | | 20 | | 30 | | 30 | | 30 | | 30 | | ns |
| R5 | t _{PHQV} | RP# to Output Delay | | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | ns |
| R6 | t _{ELQX} | CE# to Output in Low Z ⁽²⁾ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| R7 | t _{GLQX} | OE# to Output in Low Z ⁽²⁾ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| R8 | t _{EHQZ} | CE# to Output in High Z ⁽²⁾ | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | ns |
| R9 | t _{GHQZ} | OE# to Output in High Z ⁽²⁾ | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | ns |
| R10 | t _{OH} | Output Hold from Address, CE#, or OE# Change, Whichever Occurs First ⁽²⁾ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |

NOTES:

1. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.

See Figure 9, “AC Waveform: Read Operations” on page 35.

See Figure 7, “Input/Output Reference Waveform” on page 30 for timing measurements and maximum allowable input slew rate.

AC Characteristics—Read Operations, continued

| # | Sym | Parameter | Density | 32 Mbit | | | | | | | | | | | | Unit |
|-----|-------------------|---|-----------------|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------------|-----|------|
| | | | Product | 70 ns | | 90 ns | | 100 ns | | 110 ns | | | | | | |
| | | | V _{CC} | 2.7 V–3.6 V | | 2.7 V–3.6 V | | 3.0 V–3.3 V | | 2.7 V–3.3 V | | 3.0 V–3.3 V | | 2.7 V–3.3 V | | |
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| R1 | t _{AVAV} | Read Cycle Time | | 70 | | 90 | | 90 | | 100 | | 100 | | 110 | | ns |
| R2 | t _{AVQV} | Address to Output Delay | | 70 | | 90 | | 90 | | 100 | | 100 | | 110 | | ns |
| R3 | t _{ELQV} | CE# to Output Delay ⁽¹⁾ | | 70 | | 90 | | 90 | | 100 | | 100 | | 110 | | ns |
| R4 | t _{GLQV} | OE# to Output Delay ⁽¹⁾ | | 20 | | 20 | | 30 | | 30 | | 30 | | 30 | | ns |
| R5 | t _{PHQV} | RP# to Output Delay | | 150 | | 150 | | 150 | | 150 | | 150 | | 150 | | ns |
| R6 | t _{ELQX} | CE# to Output in Low Z ⁽²⁾ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | ns |
| R7 | t _{GLQX} | OE# to Output in Low Z ⁽²⁾ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | ns |
| R8 | t _{EHQZ} | CE# to Output in High Z ⁽²⁾ | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | ns |
| R9 | t _{GHQZ} | OE# to Output in High Z ⁽²⁾ | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | ns |
| R10 | t _{OH} | Output Hold from Address, CE#, or OE# Change, Whichever Occurs First ⁽²⁾ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | ns |

NOTES:

1. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.

See Figure 9, “AC Waveform: Read Operations” on page 35.

See Figure 7, “Input/Output Reference Waveform” on page 30 for timing measurements and maximum allowable input slew rate.

AC Characteristics—Read Operations, continued

| # | Sym | Parameter | Density | | 64 Mbit | | | | Unit |
|-----|-------------------|--|-----------------|------|-------------|-----|-------------|-----|------|
| | | | Product | | 80 ns | | 100 ns | | |
| | | | V _{CC} | | 2.7 V–3.6 V | | 2.7 V–3.6 V | | |
| | | | | Note | Min | Max | Min | Max | |
| R1 | t _{AVAV} | Read Cycle Time | | | 80 | | 100 | | ns |
| R2 | t _{AVQV} | Address to Output Delay | | | | 80 | | 100 | ns |
| R3 | t _{ELQV} | CE# to Output Delay | 1 | | | 80 | | 100 | ns |
| R4 | t _{GLQV} | OE# to Output Delay | 1 | | | 20 | | 20 | ns |
| R5 | t _{PHQV} | RP# to Output Delay | | | | 150 | | 150 | ns |
| R6 | t _{ELQX} | CE# to Output in Low Z | 2 | | 0 | | 0 | | ns |
| R7 | t _{GLQX} | OE# to Output in Low Z | 2 | | 0 | | 0 | | ns |
| R8 | t _{EHQZ} | CE# to Output in High Z | 2 | | | 20 | | 20 | ns |
| R9 | t _{GHQZ} | OE# to Output in High Z | 2 | | | 20 | | 20 | ns |
| R10 | t _{OH} | Output Hold from Address, CE#, or OE# Change, Whichever Occurs First | 2 | | 0 | | 0 | | ns |

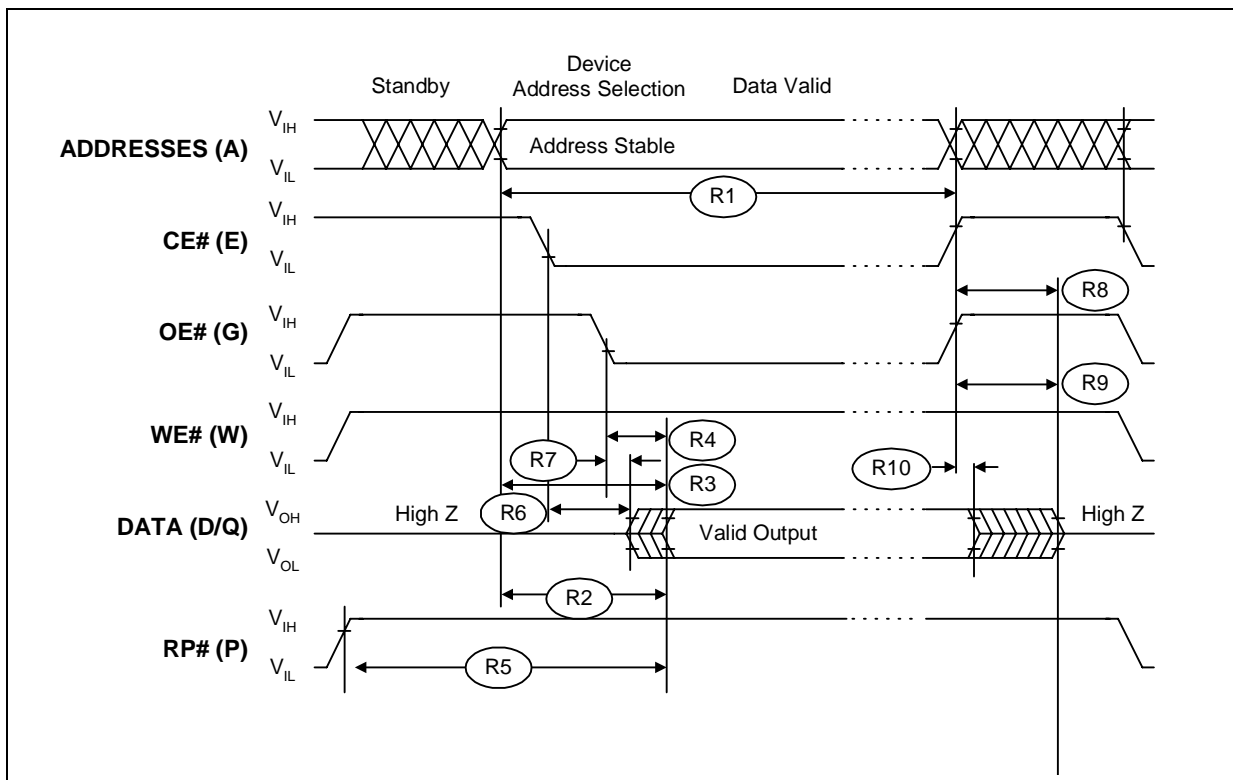
NOTES:

1. OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
2. Sampled, but not 100% tested.

See Figure 9, “AC Waveform: Read Operations” on page 35.

See Figure 7, “Input/Output Reference Waveform” on page 30 for timing measurements and maximum allowable input slew rate.

Figure 9. AC Waveform: Read Operations



4.6 AC Characteristics—Write Operations

| # | Sym | Parameter | Density | | 8 Mbit | | | | Unit |
|-----|-----------------------|---|---------------|-----|--------|-----|--------|-----|------|
| | | | Product | | 90 ns | | 110 ns | | |
| | | | 3.0 V – 3.6 V | | 80 | | 100 | | |
| | | | 2.7 V – 3.6 V | | | 90 | | 110 | |
| | | | Note | Min | Min | Min | Min | | |
| W1 | t_{PHWL} / t_{PHEL} | RP# High Recovery to WE# (CE#) Going Low | | 150 | 150 | 150 | 150 | ns | |
| W2 | t_{ELWL} / t_{WLEL} | CE# (WE#) Setup to WE# (CE#) Going Low | | 0 | 0 | 0 | 0 | ns | |
| W3 | t_{WLWH} / t_{ELEH} | WE# (CE#) Pulse Width | 1 | 50 | 60 | 70 | 70 | ns | |
| W4 | t_{DVWH} / t_{DVEH} | Data Setup to WE# (CE#) Going High | 2 | 50 | 50 | 60 | 60 | ns | |
| W5 | t_{AVWH} / t_{AVEH} | Address Setup to WE# (CE#) Going High | 2 | 50 | 60 | 70 | 70 | ns | |
| W6 | t_{WHEH} / t_{EHWH} | CE# (WE#) Hold Time from WE# (CE#) High | | 0 | 0 | 0 | 0 | ns | |
| W7 | t_{WHDX} / t_{EHDX} | Data Hold Time from WE# (CE#) High | 2 | 0 | 0 | 0 | 0 | ns | |
| W8 | t_{WHAX} / t_{EHAX} | Address Hold Time from WE# (CE#) High | 2 | 0 | 0 | 0 | 0 | ns | |
| W9 | t_{WHWL} / t_{EHEL} | WE# (CE#) Pulse Width High | 1 | 30 | 30 | 30 | 30 | ns | |
| W10 | t_{VPWH} / t_{VPEH} | V _{PP} Setup to WE# (CE#) Going High | 3 | 200 | 200 | 200 | 200 | ns | |
| W11 | t_{QVVL} | V _{PP} Hold from Valid SRD | 3 | 0 | 0 | 0 | 0 | ns | |
| W12 | t_{BHWH} / t_{BHEH} | WP# Setup to WE# (CE#) Going High | 3 | 0 | 0 | 0 | 0 | ns | |
| W13 | t_{QVBL} | WP# Hold from Valid SRD | 3 | 0 | 0 | 0 | 0 | ns | |
| W14 | t_{WHGL} | WE# High to OE# Going Low | 3 | 30 | 30 | 30 | 30 | ns | |

NOTES:

- Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low first). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
- Refer to [Table 5, "Command Bus Operations"](#) on page 15 for valid A_{IN} or D_{IN}.
- Sampled, but not 100% tested.

Write timing characteristics during erase suspend are the same as during Write-only operations. See [Figure 7, "Input/Output Reference Waveform"](#) on page 30 for timing measurements and maximum allowable input slew rate.

See [Figure 9, "AC Waveform: Read Operations"](#) on page 35.

- V_{CC}Max = 3.3 V for 32-Mbit and 64-Mbit densities.

AC Characteristics—Write Operations, continued

| # | Sym | Parameter | Density | | 16 Mbit | | | | | | Unit |
|-----|-----------------------|---|---------------|-----|---------|-------|-------|-----|--------|-----|------|
| | | | Product | | 70 ns | 80 ns | 90 ns | | 110 ns | | |
| | | | 3.0 V – 3.6 V | | | | 80 | | 100 | | |
| | | | 2.7 V – 3.6 V | | 70 | 80 | | 90 | | 110 | |
| | | | Note | Min | Min | Min | Min | Min | Min | | |
| W1 | t_{PHWL} / t_{PHEL} | RP# High Recovery to WE# (CE#) Going Low | | 150 | 150 | 150 | 150 | 150 | 150 | ns | |
| W2 | t_{ELWL} / t_{WLEL} | CE# (WE#) Setup to WE# (CE#) Going Low | | 0 | 0 | 0 | 0 | 0 | 0 | ns | |
| W3 | t_{WLWH} / t_{ELEH} | WE# (CE#) Pulse Width | 1 | 45 | 50 | 50 | 60 | 70 | 70 | ns | |
| W4 | t_{DVWH} / t_{DVEH} | Data Setup to WE# (CE#) Going High | 2 | 40 | 40 | 50 | 50 | 60 | 60 | ns | |
| W5 | t_{AVWH} / t_{AVEH} | Address Setup to WE# (CE#) Going High | 2 | 50 | 50 | 50 | 60 | 70 | 70 | ns | |
| W6 | t_{WHEH} / t_{EHWH} | CE# (WE#) Hold Time from WE# (CE#) High | | 0 | 0 | 0 | 0 | 0 | 0 | ns | |
| W7 | t_{WHDX} / t_{EHDX} | Data Hold Time from WE# (CE#) High | 2 | 0 | 0 | 0 | 0 | 0 | 0 | ns | |
| W8 | t_{WHAX} / t_{EHAX} | Address Hold Time from WE# (CE#) High | 2 | 0 | 0 | 0 | 0 | 0 | 0 | ns | |
| W9 | t_{WHWL} / t_{EHEL} | WE# (CE#) Pulse Width High | 1 | 25 | 30 | 30 | 30 | 30 | 30 | ns | |
| W10 | t_{VPWH} / t_{VPEH} | V _{PP} Setup to WE# (CE#) Going High | 3 | 200 | 200 | 200 | 200 | 200 | 200 | ns | |
| W11 | t_{QVVL} | V _{PP} Hold from Valid SRD | 3 | 0 | 0 | 0 | 0 | 0 | 0 | ns | |
| W12 | t_{BHWH} / t_{BHEH} | WP# Setup to WE# (CE#) Going High | 3 | 0 | 0 | 0 | 0 | 0 | 0 | ns | |
| W13 | t_{QVBL} | WP# Hold from Valid SRD | 3 | 0 | 0 | 0 | 0 | 0 | 0 | ns | |
| W14 | t_{WHGL} | WE# High to OE# Going Low | 3 | 30 | 30 | 30 | 30 | 30 | 30 | ns | |

NOTES:

- Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low first). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
- Refer to [Table 5, "Command Bus Operations" on page 15](#) for valid A_{IN} or D_{IN}.
- Sampled, but not 100% tested.

Write timing characteristics during erase suspend are the same as during Write-only operations. See [Figure 7, "Input/Output Reference Waveform" on page 30](#) for timing measurements and maximum allowable input slew rate.

See [Figure 9, "AC Waveform: Read Operations" on page 35](#).

- V_{CC}Max = 3.3 V for 32-Mbit and 64-Mbit densities.

AC Characteristics—Write Operations, continued

| # | Sym | Parameter | Density | 32 Mbit | | | | | | Unit |
|-----|-----------------------|---|------------------------------|---------|-------|--------|-----|--------|-----|------|
| | | | Product | 70 ns | 90 ns | 100 ns | | 110 ns | | |
| | | | 3.0 V – 3.6 V ⁽⁴⁾ | | | 90 | | 100 | | |
| | | | 2.7 V – 3.6 V ⁽⁴⁾ | 70 | 90 | | 100 | | 110 | |
| | | | Note | Min | Min | Min | Min | Min | Min | |
| W1 | t_{PHWL} / t_{PHEL} | RP# High Recovery to WE# (CE#) Going Low | | 150 | 150 | 150 | 150 | 150 | 150 | ns |
| W2 | t_{ELWL} / t_{WLEL} | CE# (WE#) Setup to WE# (CE#) Going Low | | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| W3 | t_{WLWH} / t_{ELEH} | WE# (CE#) Pulse Width | 1 | 45 | 60 | 60 | 70 | 70 | 70 | ns |
| W4 | t_{DVVH} / t_{DVEH} | Data Setup to WE# (CE#) Going High | 2 | 40 | 40 | 50 | 60 | 60 | 60 | ns |
| W5 | t_{AVWH} / t_{AVEH} | Address Setup to WE# (CE#) Going High | 2 | 50 | 60 | 60 | 70 | 70 | 70 | ns |
| W6 | t_{WHEH} / t_{EHWH} | CE# (WE#) Hold Time from WE# (CE#) High | | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| W7 | t_{WHDH} / t_{EHDX} | Data Hold Time from WE# (CE#) High | 2 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| W8 | t_{WHAX} / t_{EHAX} | Address Hold Time from WE# (CE#) High | 2 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| W9 | t_{WHWL} / t_{EHEL} | WE# (CE#) Pulse Width High | 1 | 25 | 30 | 30 | 30 | 30 | 30 | ns |
| W10 | t_{VPWH} / t_{VPEH} | V _{PP} Setup to WE# (CE#) Going High | 3 | 200 | 200 | 200 | 200 | 200 | 200 | ns |
| W11 | t_{QVVL} | V _{PP} Hold from Valid SRD | 3 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| W12 | t_{BHWL} / t_{BHEL} | WP# Setup to WE# (CE#) Going High | 3 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| W13 | t_{QVBL} | WP# Hold from Valid SRD | 3 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| W14 | t_{WHGL} | WE# High to OE# Going Low | 3 | 30 | 30 | 30 | 30 | 30 | 30 | ns |

NOTES:

- Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low first). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
- Refer to [Table 5, "Command Bus Operations"](#) on page 15 for valid A_{IN} or D_{IN} .
- Sampled, but not 100% tested.

Write timing characteristics during erase suspend are the same as during Write-only operations.
See [Figure 7, "Input/Output Reference Waveform"](#) on page 30 for timing measurements and maximum allowable input slew rate.

See [Figure 9, "AC Waveform: Read Operations"](#) on page 35.

- $V_{CCMax} = 3.3$ V for 0.25 μ m 32-Mbit devices.

AC Characteristics—Write Operations, continued

| # | Sym | Parameter | Density | 64 Mbit | | Unit | |
|-----|-----------------------|---|---------------|---------|--------|------|----|
| | | | Product | 80 ns | 100 ns | | |
| | | | 2.7 V – 3.6 V | 80 | 100 | | |
| | | | Note | Min | Min | | |
| W1 | t_{PHWL} / t_{PHEL} | RP# High Recovery to WE# (CE#) Going Low | | | 150 | 150 | ns |
| W2 | t_{ELWL} / t_{WLEL} | CE# (WE#) Setup to WE# (CE#) Going Low | | | 0 | 0 | ns |
| W3 | t_{WLWH} / t_{ELEH} | WE# (CE#) Pulse Width | 1 | | 60 | 70 | ns |
| W4 | t_{DVWH} / t_{DVEH} | Data Setup to WE# (CE#) Going High | 2 | | 40 | 40 | ns |
| W5 | t_{AVWH} / t_{AVEH} | Address Setup to WE# (CE#) Going High | 2 | | 60 | 60 | ns |
| W6 | t_{WHEH} / t_{EHWH} | CE# (WE#) Hold Time from WE# (CE#) High | | | 0 | 0 | ns |
| W7 | t_{WHDX} / t_{EHDX} | Data Hold Time from WE# (CE#) High | 2 | | 0 | 0 | ns |
| W8 | t_{WHAX} / t_{EHAX} | Address Hold Time from WE# (CE#) High | 2 | | 0 | 0 | ns |
| W9 | t_{WHWL} / t_{EHEL} | WE# (CE#) Pulse Width High | 1 | | 30 | 30 | ns |
| W10 | t_{VPWH} / t_{VPEH} | V _{PP} Setup to WE# (CE#) Going High | 3 | | 200 | 200 | ns |
| W11 | t_{QVVL} | V _{PP} Hold from Valid SRD | 3 | | 0 | 0 | ns |
| W12 | t_{BHWH} / t_{BHEH} | WP# Setup to WE# (CE#) Going High | 3 | | 0 | 0 | ns |
| W13 | t_{QVBL} | WP# Hold from Valid SRD | 3 | | 0 | 0 | ns |
| W14 | t_{WHGL} | WE# High to OE# Going Low | 3 | | 30 | 30 | ns |

NOTES:

- Write pulse width (t_{WP}) is defined from CE# or WE# going low (whichever goes low last) to CE# or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. Similarly, write pulse width high (t_{WPH}) is defined from CE# or WE# going high (whichever goes high first) to CE# or WE# going low (whichever goes low first). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
- Refer to [Table 5, “Command Bus Operations” on page 15](#) for valid A_{IN} or D_{IN}.
- Sampled, but not 100% tested.

Write timing characteristics during erase suspend are the same as during Write-only operations. See [Figure 7, “Input/Output Reference Waveform” on page 30](#) for timing measurements and maximum allowable input slew rate. See [Figure 9, “AC Waveform: Read Operations” on page 35](#).

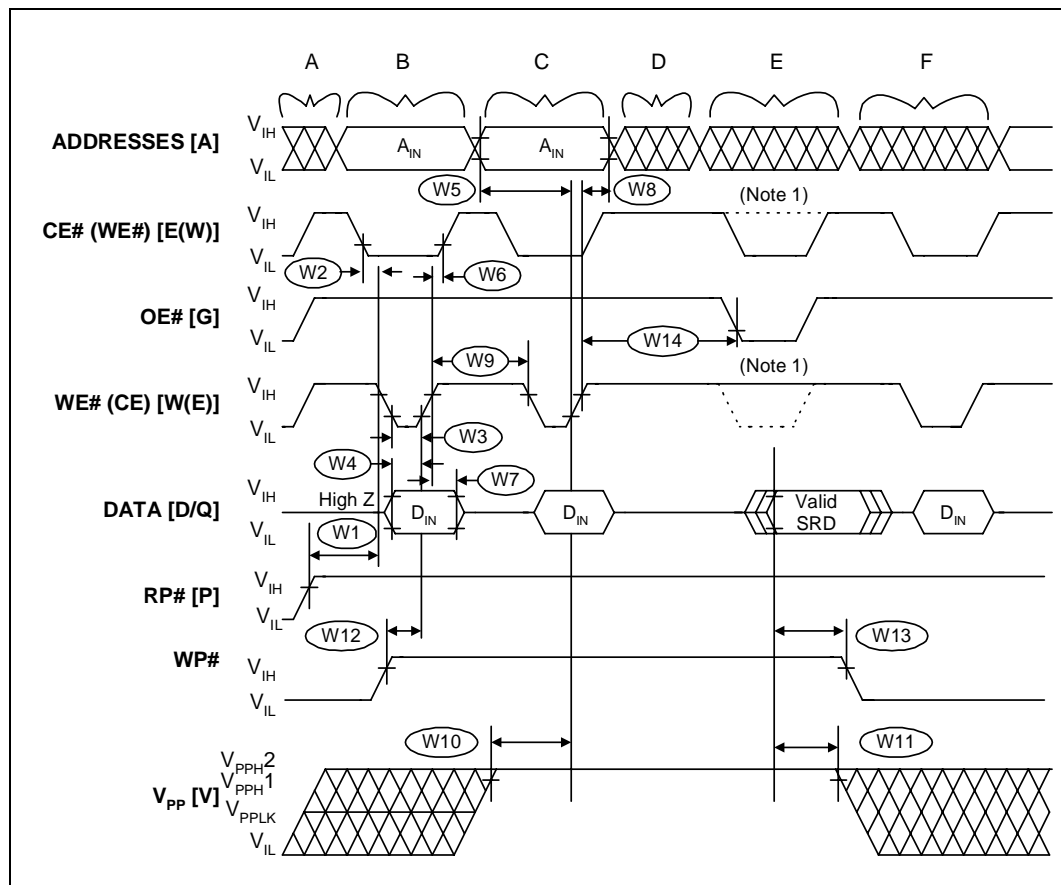
4.7 Erase and Program Timings

| Symbol | Parameter | V _{PP} | 1.65 V–3.6 V | | 11.4 V–12.6 V | | Unit |
|---|--|-----------------|--------------------|------|--------------------|------|------|
| | | Note | Typ ⁽¹⁾ | Max | Typ ⁽¹⁾ | Max | |
| t _{BWPB} | 4-KW Parameter Block Word Program Time | 2, 3 | 0.10 | 0.30 | 0.03 | 0.12 | s |
| t _{BWMB} | 32-KW Main Block Word Program Time | 2, 3 | 0.8 | 2.4 | 0.24 | 1 | s |
| t _{WHQV1} / t _{EHQV1} | Word Program Time for 0.13 and 0.18 Micron Product | 2, 3 | 12 | 200 | 8 | 185 | μs |
| | Word Program Time for 0.25 Micron Product | 2, 3 | 22 | 200 | 8 | 185 | μs |
| t _{WHQV2} / t _{EHQV2} | 4-KW Parameter Block Erase Time | 2, 3 | 0.5 | 4 | 0.4 | 4 | s |
| t _{WHQV3} / t _{EHQV3} | 32-KW Main Block Erase Time | 2, 3 | 1 | 5 | 0.6 | 5 | s |
| t _{WHRH1} / t _{EHRH1} | Program Suspend Latency | 3 | 5 | 10 | 5 | 10 | μs |
| t _{WHRH2} / t _{EHRH2} | Erase Suspend Latency | 3 | 5 | 20 | 5 | 20 | μs |

NOTES:

1. Typical values measured at T_A = +25 °C and nominal voltages.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.

Figure 10. AC Waveform: Program and Erase Operations



NOTES:

1. CE# must be toggled low when reading Status Register Data. WE# must be inactive (high) when reading Status Register Data.
- a. V_{CC} Power-Up and Standby.
 - b. Write Program or Erase Setup Command.
 - c. Write Valid Address and Data (for Program) or Erase Confirm Command.
 - d. Automated Program or Erase Delay.
 - e. Read Status Register Data (SRD): reflects completed Program/Erase operation.
 - f. Write Read Array Command.

4.8 Reset Operations

Figure 11. AC Waveform: Reset Operations

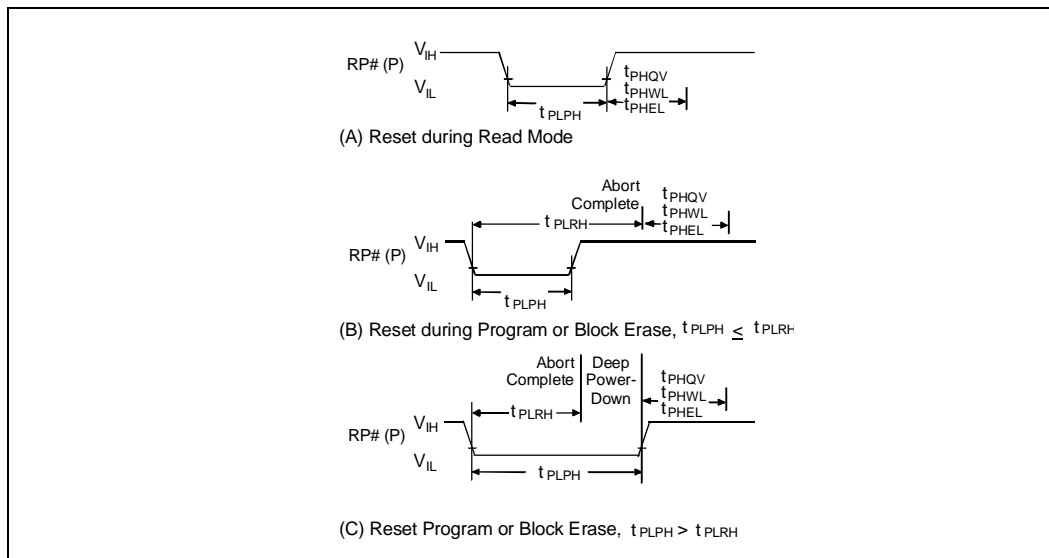


Table 11. Reset Specifications

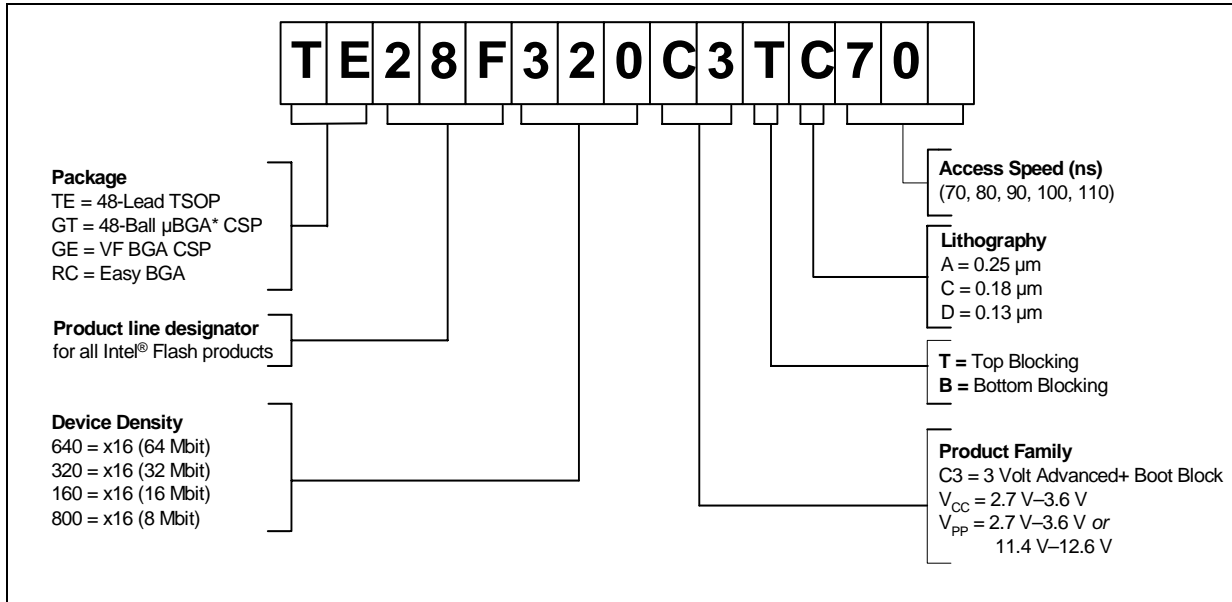
| Symbol | Parameter | Notes | $V_{CC} 2.7 V - 3.6 V$ | | Unit |
|-------------|---|-------|------------------------|-----|---------|
| | | | Min | Max | |
| t_{PLPH} | RP# Low to Reset during Read (If RP# is tied to V_{CC} , this specification is not applicable) | 2,4 | 100 | | ns |
| t_{PLRH1} | RP# Low to Reset during Block Erase | 3,4 | | 22 | μs |
| t_{PLRH2} | RP# Low to Reset during Program | 3,4 | | 12 | μs |

NOTES:

1. If t_{PLPH} is < 100 ns the device may still reset but this is not guaranteed.
2. If RP# is asserted while a Block Erase or Word Program operation is not executing, the reset will complete within 100 ns.
3. Sampled, but not 100% tested.

See Section 3.1.4 for a full description of these conditions.

5.0 Ordering Information



VALID COMBINATIONS (All Extended Temperature)

| | 48-Lead TSOP | 48-Ball μ BGA* CSP | 48-Ball VF BGA | Easy BGA |
|-------------------------|------------------------------------|------------------------------------|--|--|
| Extended 64 Mbit | TE28F640C3TC80 TE28F640C3BC80 | | GE28F640C3TC80 GE28F640C3BC80 | RC28F640C3TC80 RC28F640C3BC80 |
| | TE28F640C3TC100 TE28F640C3BC100 | | GE28F640C3TC100 GE28F640C3BC100 | RC28F640C3TC100 RC28F640C3BC100 |
| Extended 32 Mbit | TE28F320C3TC90 TE28F320C3BC90 | | GE28F320C3TD70 GE28F320C3BD70 GE28F320C3TC90 GE28F320C3BC90 | RC28F320C3TD70 RC28F320C3BD70 RC28F320C3TC90 RC28F320C3BC90 |
| | TE28F320C3TA100 TE28F320C3BA100 | GT28F320C3TA100 GT28F320C3BA100 | | RC28F320C3TA100 RC28F320C3BA100 |
| | TE28F320C3TA110 TE28F320C3BA110 | GT28F320C3TA110 GT28F320C3BA110 | | RC28F320C3TA110 RC28F320C3BA110 |
| Extended 16 Mbit | TE28F160C3TC70 TE28F160C3BC70 | | GE28F160C3TC70 GE28F160C3BC70 | RC28F160C3TC70 RC28F160C3BC70 |
| | TE28F160C3TC80 TE28F160C3BC80 | | GE28F160C3TC80 GE28F160C3BC80 | RC28F160C3TC80 RC28F160C3BC80 |
| | TE28F160C3TA90 TE28F160C3BA90 | GT28F160C3TA90 GT28F160C3BA90 | | RC28F160C3TA90 RC28F160C3BA90 |
| Extended 8 Mbit | TE28F160C3TA110 TE28F160C3BA110 | GT28F160C3TA110 GT28F160C3BA110 | | RC28F160C3TA110 RC28F160C3BA110 |
| | TE28F800C3TA90 TE28F800C3BA90 | | | RC28F800C3TA90 RC28F800C3BA90 |
| | TE28F800C3TA110 TE28F800C3BA110 | | | RC28F800C3TA110 RC28F800C3BA110 |

NOTE:



1. The second line of the 48-ball μ BGA package top side mark specifies assembly codes. For samples only, the first character signifies either "E" for engineering samples or "S" for silicon daisy chain samples. All other assembly codes without an "E" or "S" as the first character are production units.

6.0 Additional Information

| Order Number | Document/Tool |
|-----------------------------------|---|
| 297938 | <i>3 Volt Advanced+ Boot Block Flash Memory Specification Update</i> |
| 292216 | <i>AP-658 Designing for Upgrade to the Advanced+ Boot Block Flash Memory</i> |
| 292215 | <i>AP-657 Designing with the Advanced+ Boot Block Flash Memory Architecture</i> |
| Contact your Intel Representative | <i>Intel® Flash Data Integrator (IFDI) Software Developer's Kit</i> |
| 297874 | <i>IFDI Interactive: Play with Intel® Flash Data Integrator on Your PC</i> |

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at '<http://www.intel.com/design/flash>' for technical documentation and tools.



Appendix A WSM Current/Next States, Sheet 1 of 2

| Current State | SR. 7 | Data When Read | Command Input (and Next State) | | | | | | | | |
|-------------------------|-------|----------------|--|----------------------------|---------------------|---------------------|------------------------|----------------------|---------------------|----------------------|--|
| | | | Read Array (FFH) | Program Setup (10/40H) | Erase Setup (20H) | Erase Confirm (D0H) | Prog/Ers Suspend (B0H) | Prog/Ers Resume (D0) | Read Status (70H) | Clear Status (50H) | |
| Read Array | "1" | Array | Read Array | Prog. Setup | Ers. Setup | Read Array | | | Read Sts. | Read Array | |
| Read Status | "1" | Status | Read Array | Prog. Setup | Ers. Setup | Read Array | | | Read Sts. | Read Array | |
| Read Config. | "1" | Config | Read Array | Prog. Setup | Ers. Setup | Read Array | | | Read Sts. | Read Array | |
| Read Query | "1" | CFI | Read Array | Prog. Setup | Ers. Setup | Read Array | | | Read Sts. | Read Array | |
| Lock Setup | "1" | Status | Lock Command Error | | | Lock (Done) | Lock Cmd. Error | Lock (Done) | Lock Cmd. Error | | |
| Lock Cmd. Error | "1" | Status | Read Array | Prog. Setup | Ers. Setup | Read Array | | | Read Sts. | Read Array | |
| Lock Oper. (Done) | "1" | Status | Read Array | Prog. Setup | Ers. Setup | Read Array | | | Read Sts. | Read Array | |
| Prot. Prog. Setup | "1" | Status | Protection Register Program | | | | | | | | |
| Prot. Prog. (Not Done) | "0" | Status | Protection Register Program (Not Done) | | | | | | | | |
| Prot. Prog. (Done) | "1" | Status | Read Array | Prog. Setup | Ers. Setup | Read Array | | | Read Sts. | Read Array | |
| Prog. Setup | "1" | Status | Program | | | | | | | | |
| Program (Not Done) | "0" | Status | Program (Not Done) | | | | Prog. Sus. Status | Program (Not Done) | | | |
| Prog. Susp. Status | "1" | Status | Prog. Sus. Read Array | Program Suspend Read Array | | Prog. (Not Done) | Prog. Sus. Rd. Array | Program (Not Done) | Prog. Sus. Status | Prog. Sus. Rd. Array | |
| Prog. Susp. Read Array | "1" | Array | Prog. Sus. Read Array | Program Suspend Read Array | | Prog. (Not Done) | Prog. Sus. Rd. Array | Program (Not Done) | Prog. Sus. Status | Prog. Sus. Rd. Array | |
| Prog. Susp. Read Config | "1" | Config | Prog. Sus. Read Array | Program Suspend Read Array | | Prog. (Not Done) | Prog. Sus. Rd. Array | Program (Not Done) | Prog. Sus. Status | Prog. Sus. Rd. Array | |
| Prog. Susp. Read Query | "1" | CFI | Prog. Sus. Read Array | Program Suspend Read Array | | Prog. (Not Done) | Prog. Sus. Rd. Array | Program (Not Done) | Prog. Sus. Status | Prog. Sus. Rd. Array | |
| Program (Done) | "1" | Status | Read Array | Prog. Setup | Ers. Setup | Read Array | | | Read Status | Read Array | |
| Erase Setup | "1" | Status | Erase Command Error | | | Erase (Not Done) | Erase Cmd. Error | Erase (Not Done) | Erase Command Error | | |
| Erase Cmd. Error | "1" | Status | Read Array | Prog. Setup | Ers. Setup | Read Array | | | Read Status | Read Array | |
| Erase (Not Done) | "0" | Status | Erase (Not Done) | | | | Erase Sus. Status | Erase (Not Done) | | | |
| Ers. Susp. Status | "1" | Status | Erase Sus. Read Array | Prog. Setup | Ers. Sus. Rd. Array | Erase | Ers. Sus. Rd. Array | Erase | Erase Sus. Status | Ers. Sus. Rd. Array | |
| Erase Susp. Array | "1" | Array | Erase Sus. Read Array | Prog. Setup | Ers. Sus. Rd. Array | Erase | Ers. Sus. Rd. Array | Erase | Erase Sus. Status | Ers. Sus. Rd. Array | |
| Ers. Susp. Read Config | "1" | Config | Erase Sus. Read Array | Prog. Setup | Ers. Sus. Rd. Array | Erase | Ers. Sus. Rd. Array | Erase | Erase Sus. Status | Ers. Sus. Rd. Array | |
| Ers. Susp. Read Query | "1" | CFI | Erase Sus. Read Array | Prog. Setup | Ers. Sus. Rd. Array | Erase | Ers. Sus. Rd. Array | Erase | Erase Sus. Status | Ers. Sus. Rd. Array | |
| Erase (Done) | "1" | Status | Read Array | Prog. Setup | Ers. Setup | Read Array | | | Read Sts. | Read Array | |

Appendix A: WSM Current/Next States, Sheet 2 of 2

| Current State | Command Input (and Next State) | | | | | | |
|--------------------------|--|--------------------------|----------------------------|--------------------------|-----------------------|-------------------------|----------------------|
| | Read Config (90H) | Read Query (98H) | Lock Setup (60H) | Prot. Prog. Setup (C0H) | Lock Confirm (01H) | Lock Down Confirm (2FH) | Unlock Confirm (D0H) |
| Read Array | Read Config. | Read Query | Lock Setup | Prot. Prog. Setup | Read Array | | |
| Read Status | Read Config. | Read Query | Lock Setup | Prot. Prog. Setup | Read Array | | |
| Read Config. | Read Config. | Read Query | Lock Setup | Prot. Prog. Setup | Read Array | | |
| Read Query | Read Config. | Read Query | Lock Setup | Prot. Prog. Setup | Read Array | | |
| Lock Setup | Locking Command Error | | | | Lock Operation (Done) | | |
| Lock Cmd. Error | Read Config. | Read Query | Lock Setup | Prot. Prog. Setup | Read Array | | |
| Lock Oper. (Done) | Read Config. | Read Query | Lock Setup | Prot. Prog. Setup | Read Array | | |
| Prot. Prog. Setup | Protection Register Program | | | | | | |
| Prot. Prog. (Not Done) | Protection Register Program (Not Done) | | | | | | |
| Prot. Prog. (Done) | Read Config. | Read Query | Lock Setup | Prot. Prog. Setup | Read Array | | |
| Prog. Setup | Program | | | | | | |
| Program (Not Done) | Program (Not Done) | | | | | | |
| Prog. Susp. Status | Prog. Susp. Read Config. | Prog. Susp. Read Query | Program Suspend Read Array | | | | Program (Not Done) |
| Prog. Susp. Read Array | Prog. Susp. Read Config. | Prog. Susp. Read Query | Program Suspend Read Array | | | | Program (Not Done) |
| Prog. Susp. Read Config. | Prog. Susp. Read Config. | Prog. Susp. Read Query | Program Suspend Read Array | | | | Program (Not Done) |
| Prog. Susp. Read Query. | Prog. Susp. Read Config. | Prog. Susp. Read Query | Program Suspend Read Array | | | | Program (Not Done) |
| Program (Done) | Read Config. | Read Query | Lock Setup | Prot. Prog. Setup | Read Array | | |
| Erase Setup | Erase Command Error | | | | | Erase (Not Done) | |
| Erase Cmd. Error | Read Config. | Read Query | Lock Setup | Prot. Prog. Setup | Read Array | | |
| Erase (Not Done) | Erase (Not Done) | | | | | | |
| Erase Susp. Status | Ers. Susp. Read Config. | Erase Suspend Read Query | Lock Setup | Erase Suspend Read Array | | | Erase (Not Done) |
| Erase Suspend Array | Ers. Susp. Read Config. | Erase Suspend Read Query | Lock Setup | Erase Suspend Read Array | | | Erase (Not Done) |
| Eras Sus. Read Config | Erase Suspend Read Config. | Erase Suspend Read Query | Lock Setup | Erase Suspend Read Array | | | Erase (Not Done) |
| Eras Sus. Read Query | Erase Suspend Read Config. | Erase Suspend Read Query | Lock Setup | Erase Suspend Read Array | | | Erase (Not Done) |
| Ers.(Done) | Read Config. | Read Query | Lock Setup | Prot. Prog. Setup | Read Array | | |

Appendix B Program/Erase Flowcharts

Figure 12. Automated Word Programming Flowchart

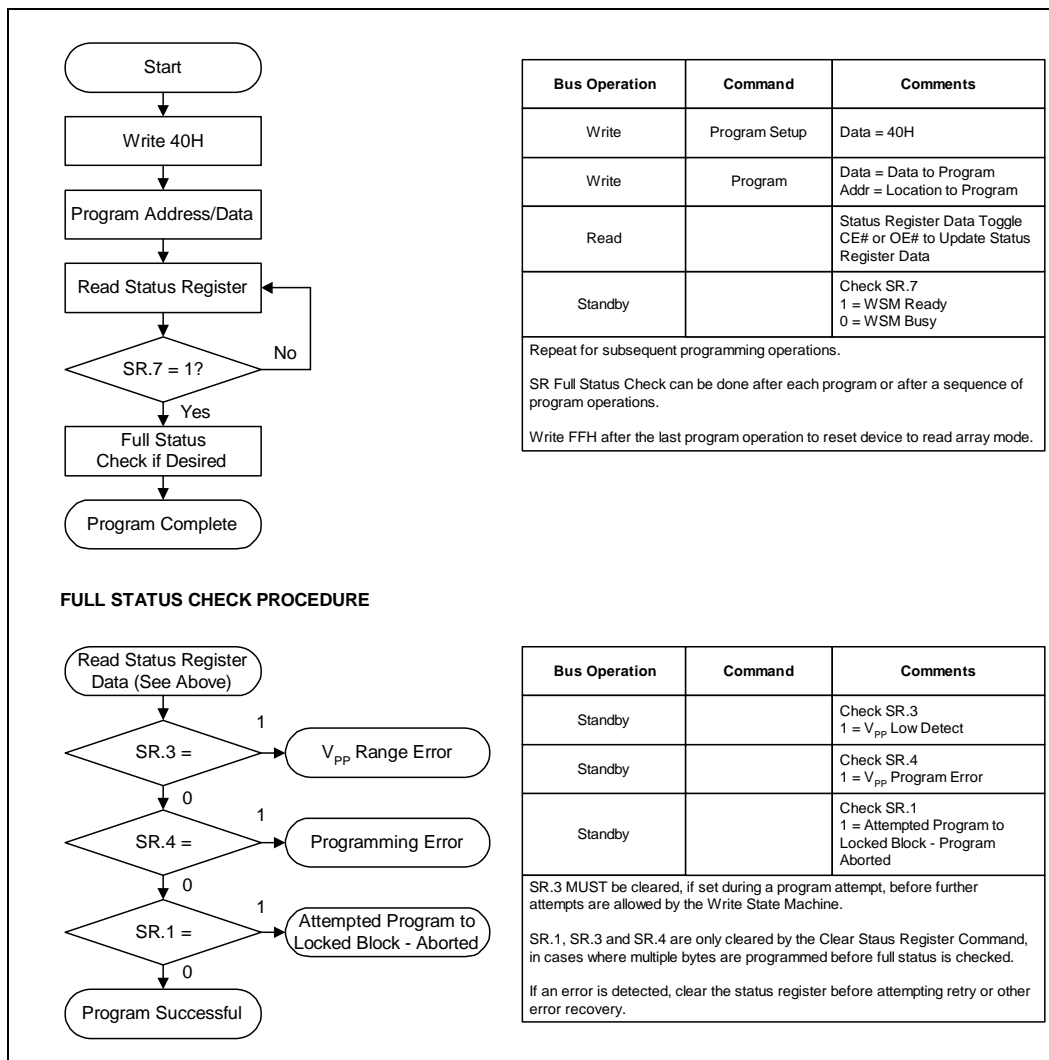


Figure 13. Program Suspend/Resume Flowchart

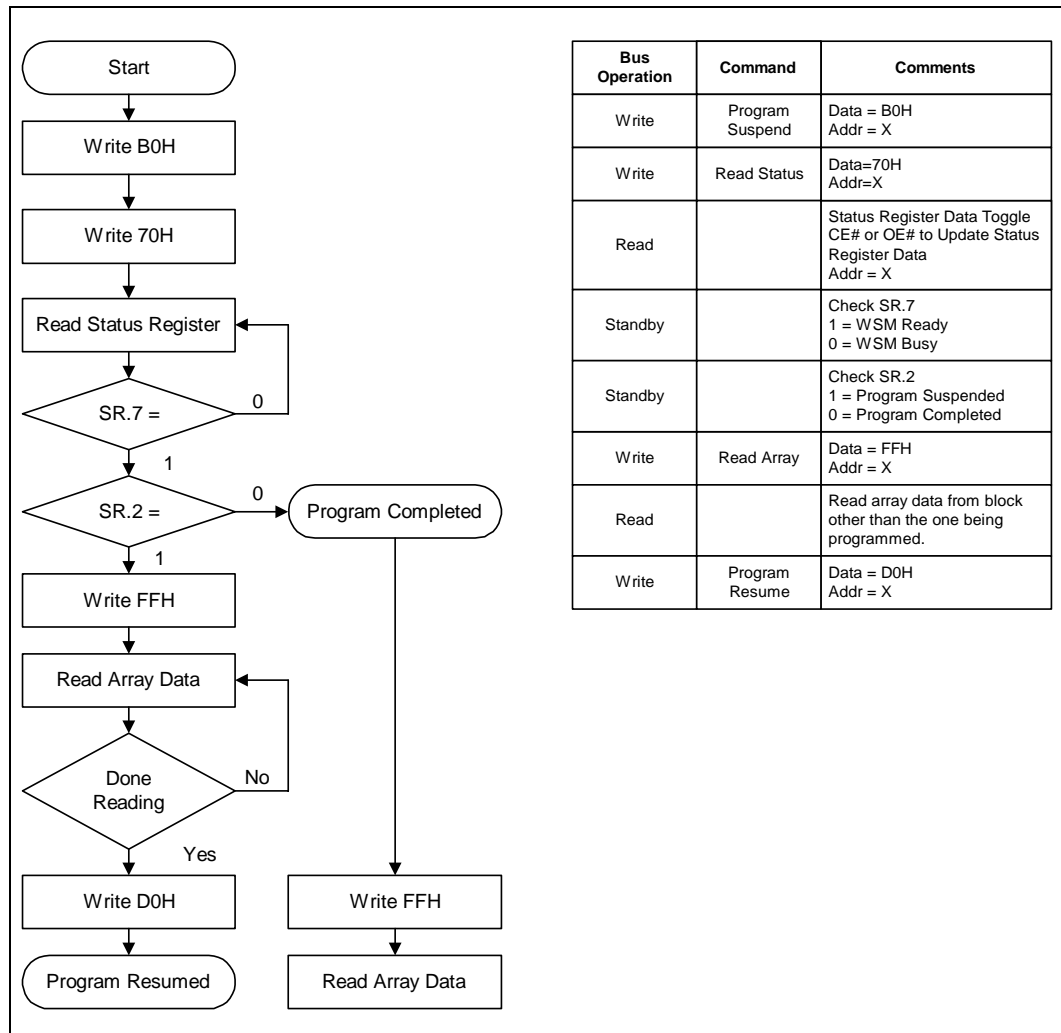


Figure 14. Automated Block Erase Flowchart

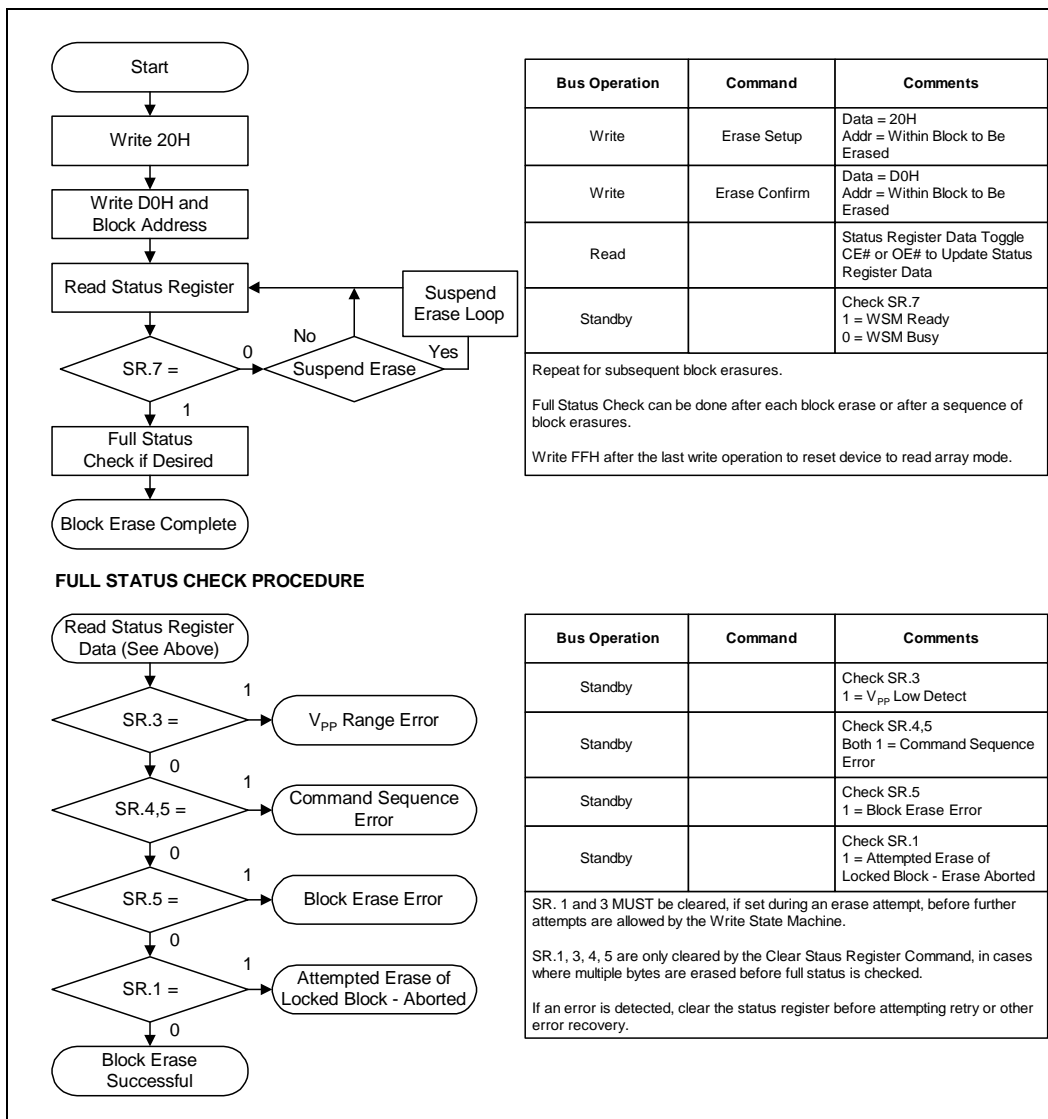


Figure 15. Erase Suspend/Resume Flowchart

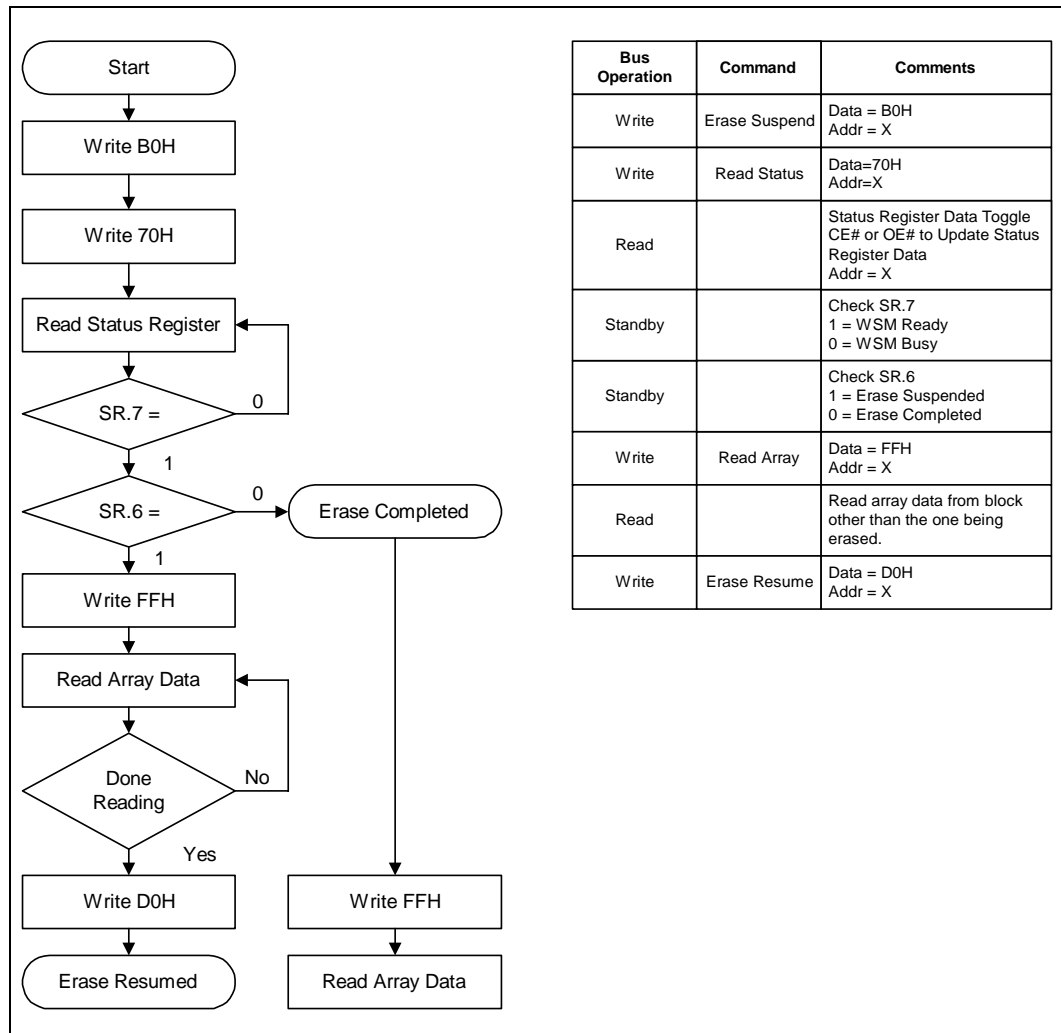


Figure 16. Locking Operations Flowchart

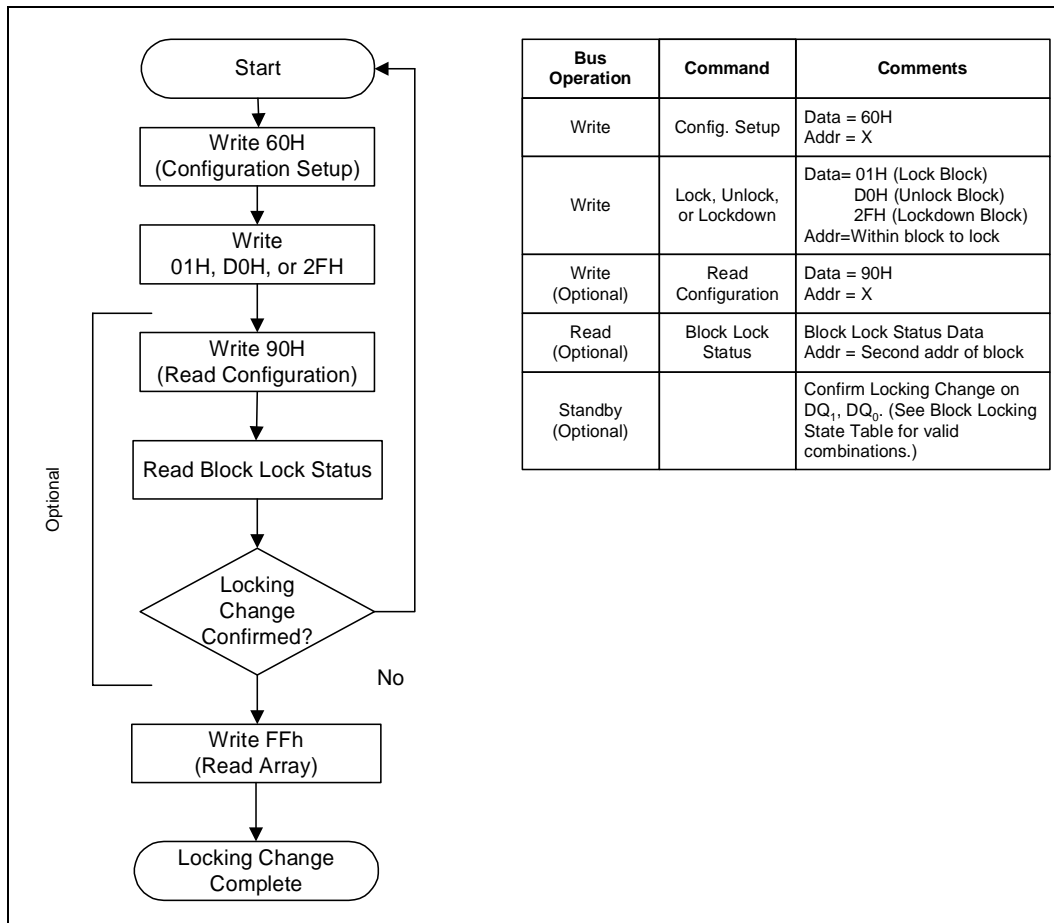
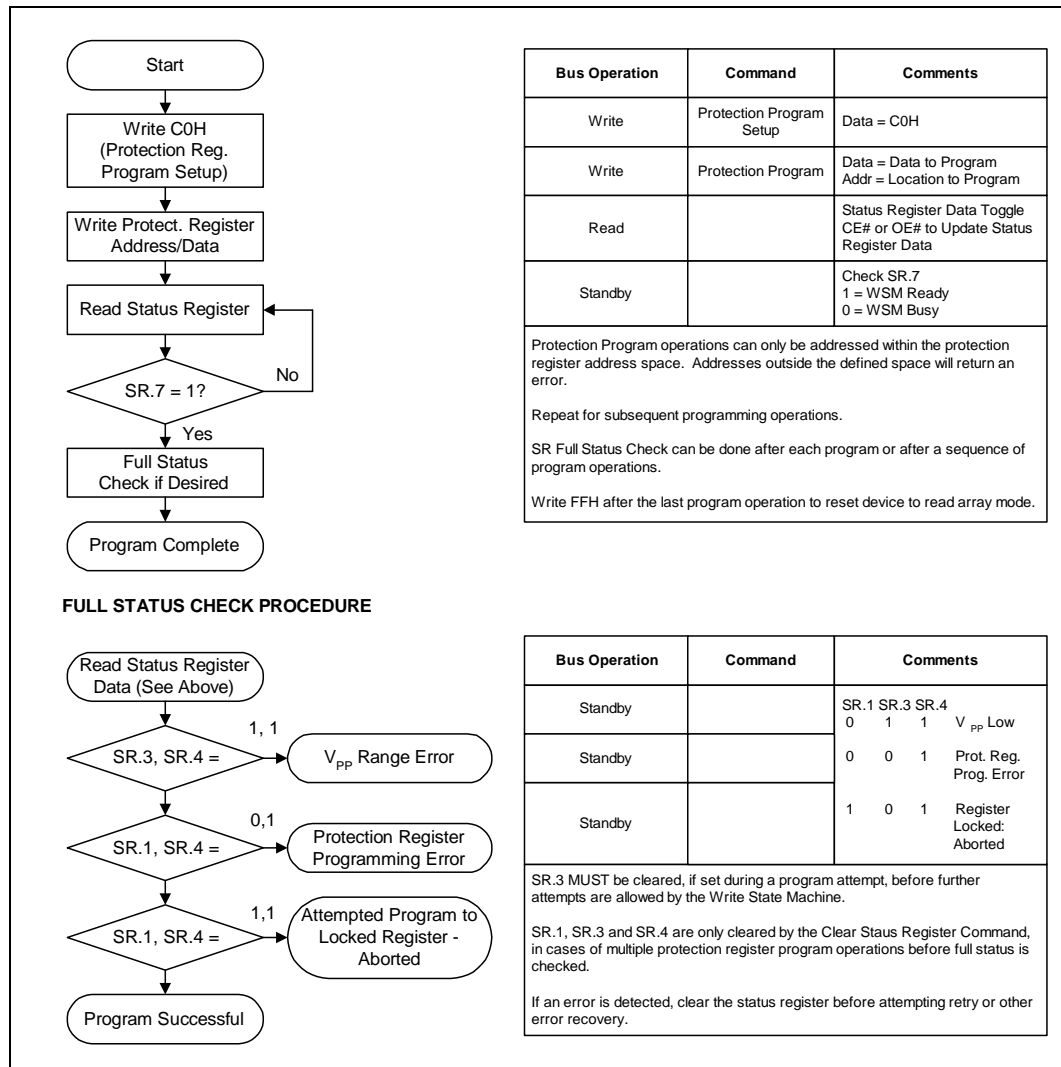


Figure 17. Protection Register Programming Flowchart



Appendix C Common Flash Interface Query Structure

This appendix defines the data structure or “database” returned by the Common Flash Interface (CFI) Query command. System software should parse this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. Once this information has been obtained, the software will know which command sets to use to enable flash writes, block erases, and otherwise control the flash component. The Query is part of an overall specification for multiple command set and control-interface descriptions called Common Flash Interface, or CFI.

C.1 Query Structure Output

The Query “database” allows system software to gain information for controlling the flash component. This section describes the device’s CFI-compliant interface that allows the host system to access Query data.

Query data are always presented on the lowest order data outputs (DQ₀₋₇) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the Query table device starting address is a 10h, which is a word address for x16 devices.

For a word-wide (x16) device, the first two bytes of the Query structure, “Q” and “R” in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00H data on upper bytes. Thus, the device outputs ASCII “Q” in the low byte (DQ₀₋₇) and 00h in the high byte (DQ₈₋₁₅).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the “h” suffix has been dropped. In addition, since the upper byte of word-wide devices is always “00h,” the leading “00” has been dropped from the table notation and only the lower byte value is shown. Any x16 device outputs can be assumed to have 00h on the upper byte in this mode.

Table 12. Summary of Query Structure Output As a Function of Device and Mode

| Device | Hex Offset | Code | ASCII Value |
|------------------|------------|------|-------------|
| Device Addresses | 10: | 51 | “Q” |
| | 11: | 52 | “R” |
| | 12: | 59 | “Y” |

Table 13. Example of Query Structure Output of x16 and x8 Devices

| Word Addressing | | | Byte Addressing | | |
|---------------------------------|---------------------------------|-----------|--------------------------------|--------------------------------|----------|
| Offset | Hex Code | Value | Offset | Hex Code | Value |
| A ₁₅ –A ₀ | D ₁₅ –D ₀ | | A ₇ –A ₀ | D ₇ –D ₀ | |
| 0010h | 0051 | “Q” | 10h | 51 | “Q” |
| 0011h | 0052 | “R” | 11h | 52 | “R” |
| 0012h | 0059 | “Y” | 12h | 59 | “Y” |
| 0013h | P_ID _{LO} | PrVendor | 13h | P_ID _{LO} | PrVendor |
| 0014h | P_ID _{HI} | ID # | 14h | P_ID _{LO} | ID # |
| 0015h | P _{LO} | PrVendor | 15h | P_ID _{HI} | ID # |
| 0016h | P _{HI} | TblAdr | 16h | ... | ... |
| 0017h | A_ID _{LO} | AltVendor | 17h | | |
| 0018h | A_ID _{HI} | ID # | 18h | | |
| ... | ... | ... | ... | | |

C.2 Query Structure Overview

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or “database.” The structure sub-sections and address locations are summarized below.

Table 14. Query Structure⁽¹⁾

| Offset | Sub-Section Name | Description |
|------------------------|---|--|
| 00h | | Manufacturer Code |
| 01h | | Device Code |
| (BA+2)h ⁽²⁾ | Block Status Register | Block-Specific Information |
| 04-0Fh | Reserved | Reserved for Vendor-Specific Information |
| 10h | CFI Query Identification String | Command Set ID and Vendor Data Offset |
| 1Bh | System Interface Information | Device Timing and Voltage Information |
| 27h | Device Geometry Definition | Flash Device Layout |
| P ⁽³⁾ | Primary Intel-Specific Extended Query Table | Vendor-Defined Additional Information Specific to the Primary Vendor Algorithm |

NOTES:

1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of device bus width and mode.
2. BA = The beginning location of a Block Address (e.g., 08000h is the beginning location of block 1 when the block size is 32 Kword).
3. Offset 15 defines “P” which points to the Primary Intel-specific Extended Query Table.

C.3 Block Lock Status Register

The block-status register indicates whether an Erase operation completed successfully or whether a given block is locked or can be accessed for flash Program/Erase operations.

Block Erase Status (BSR.1) allows system software to determine the success of the last Block Erase operation. BSR.1 can be used just after power-up to verify that the V_{CC} supply was not accidentally removed during an Erase operation. This bit is reset only by issuing another Erase operation to the block. The block-status register is accessed from word address 02h within each block.

Table 15. Block Status Register

| Offset | Length | Description | Add. | Value |
|------------------------|--------|--|-------|-----------------|
| (BA+2)h ⁽¹⁾ | 1 | Block Lock Status Register | BA+2: | --00 or --01 |
| | | BSR.0 Block Lock Status 0 = Unlocked 1 = Locked | BA+2: | (bit 0): 0 or 1 |
| | | BSR.1 Block Lock-Down Status 0 = Not locked down 1 = Locked down | BA+2: | (bit 1): 0 or 1 |
| | | BSR 2–7: <i>Reserved for future use</i> | BA+2: | (bit 2–7): 0 |

NOTE:

1. BA = The beginning location of a Block Address (i.e., 008000h is the beginning location of block 1 in word mode.)

C.4 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table 16. CFI Identification

| Offset | Length | Description | Add. | Hex Code | Value |
|--------|--------|---|-------------------|----------------------|-------------------|
| 10h | 3 | Query-unique ASCII string "QRY" | 10: 11: 12: | --51 --52 --59 | "Q" "R" "Y" |
| 13h | 2 | Primary vendor command set and control interface ID code 16-bit ID code for vendor-specified algorithms | 13: 14: | --03 --00 | |
| 15h | 2 | Extended Query Table primary algorithm address | 15: 16: | --35 --00 | |
| 17h | 2 | Alternate vendor command set and control interface ID code 0000h means no second vendor-specified algorithm exists | 17: 18: | --00 --00 | |
| 19h | 2 | Secondary algorithm Extended Query Table address 0000h means none exists | 19: 1A: | --00 --00 | |

C.5 System Interface Information

Table 17. System Interface Information

| Offset | Length | Description | Add. | Hex Code | Value |
|--------|--------|---|------|----------|--------|
| 1Bh | 1 | V _{CC} logic supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts | 1B: | --27 | 2.7 V |
| 1Ch | 1 | V _{CC} logic supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts | 1C: | --36 | 3.6 V |
| 1Dh | 1 | V _{PP} [programming] supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts | 1D: | --B4 | 11.4 V |
| 1Eh | 1 | V _{PP} [programming] supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts | 1E: | --C6 | 12.6 V |
| 1Fh | 1 | "n" such that typical single word program time-out = 2 ⁿ μs | 1F: | --05 | 32 μs |
| 20h | 1 | "n" such that typical max. buffer write time-out = 2 ⁿ μs | 20: | --00 | NA |
| 21h | 1 | "n" such that typical block erase time-out = 2 ⁿ ms | 21: | --0A | 1 s |
| 22h | 1 | "n" such that typical full chip erase time-out = 2 ⁿ ms | 22: | --00 | NA |
| 23h | 1 | "n" such that maximum word program time-out = 2 ⁿ times typical | 23: | --04 | 512μs |
| 24h | 1 | "n" such that maximum buffer write time-out = 2 ⁿ times typical | 24: | --00 | NA |
| 25h | 1 | "n" such that maximum block erase time-out = 2 ⁿ times typical | 25: | --03 | 8s |
| 26h | 1 | "n" such that maximum chip erase time-out = 2 ⁿ times typical | 26: | --00 | NA |

C.6 Device Geometry Definition

Table 18. Device Geometry Definition

| Offset | Length | Description | Code See table below | | |
|--------|--------|---|-------------------------|------|-----|
| 27h | 1 | "n" such that device size = 2 ⁿ in number of bytes | 27: | | |
| 28h | 2 | Flash device interface: <u>x8 async</u> <u>x16 async</u> <u>x8/x16 async</u> 28:00,29:00 28:01,29:00 28:02,29:00 | 28: | --01 | x16 |
| | | | 29: | --00 | |
| 2Ah | 2 | "n" such that maximum number of bytes in write buffer = 2 ⁿ | 2A: | --00 | 0 |
| | | | 2B: | --00 | |
| 2Ch | 1 | Number of erase block regions within device: 1. x = 0 means no erase blocking; the device erases in "bulk" 2. x specifies the number of device or partition regions with one or more contiguous same-size erase blocks. 3. Symmetrically blocked partitions have one blocking region 4. Partition size = (total blocks) x (individual block size) | 2C: | --02 | 2 |
| 2Dh | 4 | Erase Block Region 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes | 2D: | | |
| | | | 2E: | | |
| | | | 2F: | | |
| | | | 30: | | |
| 31h | 4 | Erase Block Region 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes | 31: | | |
| | | | 32: | | |
| | | | 33: | | |
| | | | 34: | | |

| Device Geometry Definition | | | | | | | | |
|----------------------------|--------|------|---------|------|---------|------|---------|------|
| Address | 8 Mbit | | 16 Mbit | | 32 Mbit | | 64 Mbit | |
| | -B | -T | -B | -T | -B | -T | -B | -T |
| 27: | --14 | --14 | --15 | --15 | --16 | --16 | --17 | --17 |
| 28: | --01 | --01 | --01 | --01 | --01 | --01 | --01 | --01 |
| 29: | --00 | --00 | --00 | --00 | --00 | --00 | --00 | --00 |
| 2A: | --00 | --00 | --00 | --00 | --00 | --00 | --00 | --00 |
| 2B: | --00 | --00 | --00 | --00 | --00 | --00 | --00 | --00 |
| 2C: | --02 | --02 | --02 | --02 | --02 | --02 | --02 | --02 |
| 2D: | --07 | --0E | --07 | --1E | --07 | --3E | --07 | --7E |
| 2E: | --00 | --00 | --00 | --00 | --00 | --00 | --00 | --00 |
| 2F: | --20 | --00 | --20 | --00 | --20 | --00 | --20 | --00 |
| 30: | --00 | --01 | --00 | --01 | --00 | --01 | --00 | --01 |
| 31: | --0E | --07 | --1E | --07 | --3E | --07 | --7E | --07 |
| 32: | --00 | --00 | --00 | --00 | --00 | --00 | --00 | --00 |
| 33: | --00 | --20 | --00 | --20 | --00 | --20 | --00 | --20 |
| 34: | --01 | --00 | --01 | --00 | --01 | --00 | --01 | --00 |

C.7 Intel-Specific Extended Query Table

Certain flash features and commands are optional. The Intel-Specific Extended Query table specifies this and other similar types of information.

Table 19. Primary-Vendor Specific Extended Query

| Offset(1) P = 35h | Length | Description (Optional Flash Features and Commands) | Address | Hex Code | Value |
|--------------------------------------|--------|---|---|--|-------------------|
| (P+0)h (P+1)h (P+2)h | 3 | Primary extended query table Unique ASCII string "PRI" | 35: 36: 37: | --50 --52 --49 | "P" "R" "I" |
| (P+3)h | 1 | Major version number, ASCII | 38: | --31 | "1" |
| (P+4)h | 1 | Minor version number, ASCII | 39: | --30 | "0" |
| (P+5)h (P+6)h (P+7)h (P+8)h | 4 | Optional feature and command support (1=yes, 0=no) bits 9–31 are reserved; undefined bits are "0." If bit 31 is "1" then another 31 bit field of optional features follows at the end of the bit-30 field. | 3A: 3B: 3C: 3D: | --66 --00 --00 --00 | |
| | | bit 0 Chip erase supported bit 1 Suspend erase supported bit 2 Suspend program supported bit 3 Legacy lock/unlock supported bit 4 Queued erase supported bit 5 Instant individual block locking supported bit 6 Protection bits supported bit 7 Page mode read supported bit 8 Synchronous read supported | bit 0 = 0 bit 1 = 1 bit 2 = 1 bit 3 = 0 bit 4 = 0 bit 5 = 1 bit 6 = 1 bit 7 = 0 bit 8 = 0 | No Yes Yes No No Yes Yes No No | |
| (P+9)h | 1 | Supported functions after suspend: Read Array, Status, Query Other supported operations are: <i>bits 1–7 reserved; undefined bits are "0"</i> | 3E: | --01 | |
| | | bit 0 Program supported after erase suspend | bit 0 = 1 | | Yes |
| (P+A)h (P+B)h | 2 | Block status register mask bits 2–15 are Reserved; undefined bits are "0" bit 0 Block Lock-Bit Status Register active bit 1 Block Lock-Down Bit Status active | 3F: 40: | --03 --00 | |
| | | | bit 0 = 1 bit 1 = 1 | Yes Yes | |
| (P+C)h | 1 | V _{CC} logic supply highest performance program/erase voltage bits 0–3 BCD value in 100 mV bits 4–7 BCD value in volts | 41: | --33 | 3.3 V |
| (P+D)h | 1 | V _{PP} optimum program/erase supply voltage bits 0–3 BCD value in 100 mV bits 4–7 HEX value in volts | 42: | --C0 | 12.0 V |

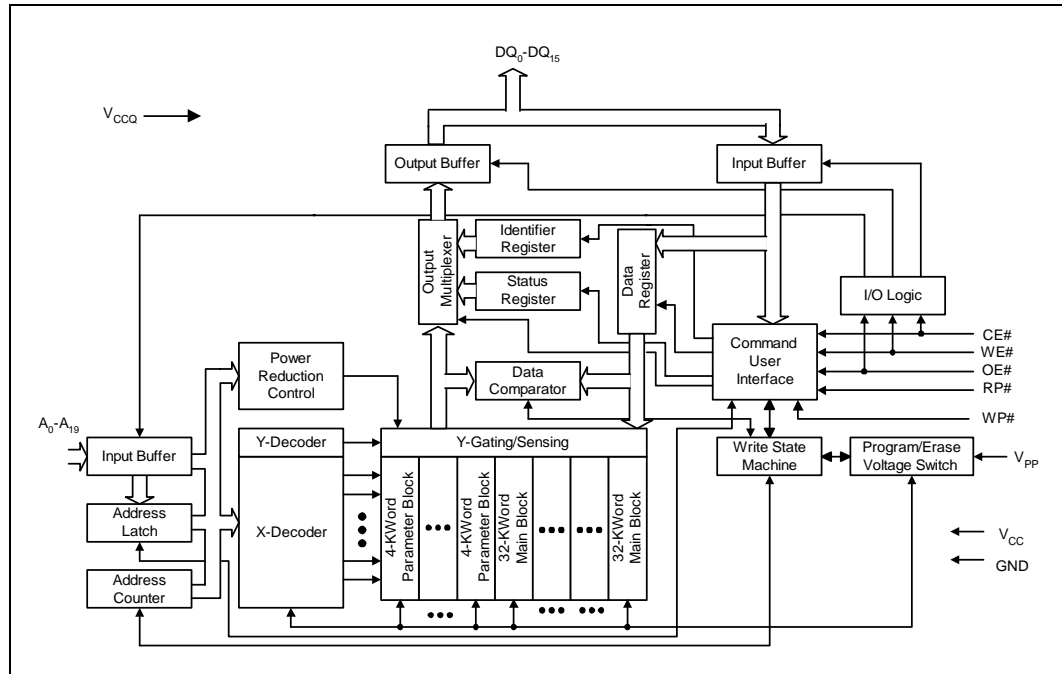
Table 20. Protection Register Information

| Offset(1) P = 35h | Length | Description (Optional Flash Features and Commands) | Address | Hex Code | Value |
|------------------------------|--------|---|-------------------|----------------------|----------------------|
| (P+E)h | 1 | Number of Protection register fields in JEDEC ID space. "00h," indicates that 256 protection bytes are available | 43: | --01 | 01 |
| (P+F)h (P+10)h (P+11)h | 4 | Protection Field 1: Protection Description This field describes user-available One Time Programmable (OTP) Protection register bytes. Some are pre-programmed with device-unique serial numbers. Others are user programmable. Bits 0–15 point to the Protection register Lock byte, the section's first byte. The following bytes are factory pre-programmed and user-programmable. bits 0–7 = Lock/bytes JEDEC-plane physical low address bits 8–15 = Lock/bytes JEDEC -plane physical high address bits 16–23 = "n" such that 2 ⁿ = factory pre-programmed bytes bits 24–31 = "n" such that 2 ⁿ = user programmable bytes | 44: 45: 46: | --80 --00 --03 | 80h 00h 8 byte |
| (P+12)h | | 47: | --03 | 8 byte | |
| (P+13)h | | Reserved for future use | 48: | | |

NOTE:

1. The variable P is a pointer which is defined at CFI offset 15h.

Appendix D Architecture Block Diagram





Appendix E Word-Wide Memory Map Diagrams

| 8-Mbit Word-Wide Memory Addressing | | | | | | | |
|------------------------------------|-------------|--|--|-------------|-------------|--|--|
| Top Boot | | | | Bottom Boot | | | |
| Size (KW) | 8 Mbit | | | Size (KW) | 8 Mbit | | |
| 4 | 7F000-7FFFF | | | 32 | 78000-7FFFF | | |
| 4 | 7E000-7EFFF | | | 32 | 70000-77FFF | | |
| 4 | 7D000-7DFFF | | | 32 | 68000-6FFFF | | |
| 4 | 7C000-7CFFF | | | 32 | 60000-67FFF | | |
| 4 | 7B000-7BFFF | | | 32 | 58000-5FFFF | | |
| 4 | 7A000-7AFFF | | | 32 | 50000-57FFF | | |
| 4 | 79000-79FFF | | | 32 | 48000-4FFFF | | |
| 4 | 78000-78FFF | | | 32 | 40000-47FFF | | |
| 32 | 70000-77FFF | | | 32 | 38000-3FFFF | | |
| 32 | 68000-6FFFF | | | 32 | 30000-37FFF | | |
| 32 | 60000-67FFF | | | 32 | 28000-2FFFF | | |
| 32 | 58000-5FFFF | | | 32 | 20000-27FFF | | |
| 32 | 50000-57FFF | | | 32 | 18000-1FFFF | | |
| 32 | 48000-4FFFF | | | 32 | 10000-17FFF | | |
| 32 | 40000-47FFF | | | 32 | 08000-0FFFF | | |
| 32 | 38000-3FFFF | | | 4 | 07000-07FFF | | |
| 32 | 30000-37FFF | | | 4 | 06000-06FFF | | |
| 32 | 28000-2FFFF | | | 4 | 05000-05FFF | | |
| 32 | 20000-27FFF | | | 4 | 04000-04FFF | | |
| 32 | 18000-1FFFF | | | 4 | 03000-03FFF | | |
| 32 | 10000-17FFF | | | 4 | 02000-02FFF | | |
| 32 | 08000-0FFFF | | | 4 | 01000-01FFF | | |
| 32 | 00000-07FFF | | | 4 | 00000-00FFF | | |



| 16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing | | | | | | | |
|---|-------------|---------------|----------------|-------------|---------|---------|----------------|
| Top Boot | | | | Bottom Boot | | | |
| Size (KW) | 16 Mbit | 32 Mbit | 64 Mbit | Size (KW) | 16 Mbit | 32 Mbit | 64 Mbit |
| 4 | FF000-FFFFF | 1FF000-1FFFFF | 3FF000-3FFFFFF | 32 | | | 3F8000-3FFFFFF |
| 4 | FE000-FEFFF | 1FE000-1FEFFF | 3FE000-3FEFFF | 32 | | | 3F0000-3F7FFF |
| 4 | FD000-FDFFF | 1FD000-1FDFFF | 3FD000-3FDFFF | 32 | | | 3E8000-3EFFFF |
| 4 | FC000-FCFFF | 1FC000-1FCFFF | 3FC000-3FCFFF | 32 | | | 3E0000-3E7FFF |
| 4 | FB000-FBFFF | 1FB000-1FBFFF | 3FB000-3FBFFF | 32 | | | 3D8000-3DFFFF |
| 4 | FA000-FAFFF | 1FA000-1FAFFF | 3FA000-3FAFFF | 32 | | | 3D0000-3D7FFF |
| 4 | F9000-F9FFF | 1F9000-1F9FFF | 3F9000-3F9FFF | 32 | | | 3C8000-3CFFFF |
| 4 | F8000-F8FFF | 1F8000-1F8FFF | 3F8000-3F8FFF | 32 | | | 3C0000-3C7FFF |
| 32 | F0000-F7FFF | 1F0000-1F7FFF | 3F0000-3F7FFF | 32 | | | 3B8000-3BFFFF |
| 32 | E8000-EFFFF | 1E8000-1EFFFF | 3E8000-3EFFFF | 32 | | | 3B0000-3B7FFF |
| 32 | E0000-E7FFF | 1E0000-1E7FFF | 3E0000-3E7FFF | 32 | | | 3A8000-3AFFFF |
| 32 | D8000-DFFFF | 1D8000-1DFFFF | 3D8000-3DFFFF | 32 | | | 3A0000-3A7FFF |
| 32 | D0000-D7FFF | 1D0000-1D7FFF | 3D0000-3D7FFF | 32 | | | 398000-39FFFF |
| 32 | C8000-CFFFF | 1C8000-1CFFFF | 3C8000-3CFFFF | 32 | | | 390000-397FFF |
| 32 | C0000-C7FFF | 1C0000-1C7FFF | 3C0000-3C7FFF | 32 | | | 388000-38FFFF |
| 32 | B8000-BFFFF | 1B8000-1BFFFF | 3B8000-3BFFFF | 32 | | | 380000-387FFF |
| 32 | B0000-B7FFF | 1B0000-1B7FFF | 3B0000-3B7FFF | 32 | | | 378000-37FFFF |
| 32 | A8000-AFFFF | 1A8000-1AFFFF | 3A8000-3AFFFF | 32 | | | 370000-377FFF |
| 32 | A0000-A7FFF | 1A0000-1A7FFF | 3A0000-3A7FFF | 32 | | | 368000-36FFFF |
| 32 | 98000-9FFFF | 198000-19FFFF | 398000-39FFFF | 32 | | | 360000-367FFF |
| 32 | 90000-97FFF | 190000-197FFF | 390000-397FFF | 32 | | | 358000-35FFFF |
| 32 | 88000-8FFFF | 188000-18FFFF | 388000-38FFFF | 32 | | | 350000-357FFF |
| 32 | 80000-87FFF | 180000-187FFF | 380000-387FFF | 32 | | | 348000-34FFFF |
| 32 | 78000-77FFF | 178000-177FFF | 378000-377FFF | 32 | | | 340000-347FFF |
| 32 | 70000-77FFF | 170000-177FFF | 370000-377FFF | 32 | | | 338000-33FFFF |
| 32 | 68000-6FFFF | 168000-16FFFF | 368000-36FFFF | 32 | | | 330000-337FFF |
| 32 | 60000-67FFF | 160000-167FFF | 360000-367FFF | 32 | | | 328000-32FFFF |
| 32 | 58000-5FFFF | 158000-15FFFF | 358000-35FFFF | 32 | | | 320000-327FFF |
| 32 | 50000-57FFF | 150000-157FFF | 350000-357FFF | 32 | | | 318000-31FFFF |
| 32 | 48000-4FFFF | 148000-14FFFF | 348000-34FFFF | 32 | | | 310000-317FFF |
| 32 | 40000-47FFF | 140000-147FFF | 340000-347FFF | 32 | | | 308000-30FFFF |
| 32 | 38000-3FFFF | 138000-13FFFF | 338000-33FFFF | 32 | | | 300000-307FFF |
| 32 | 30000-37FFF | 130000-137FFF | 330000-337FFF | 32 | | | 2F8000-2FFFFF |
| 32 | 28000-2FFFF | 128000-12FFFF | 328000-32FFFF | 32 | | | 2F0000-2F7FFF |
| 32 | 20000-27FFF | 120000-127FFF | 320000-327FFF | 32 | | | 2E8000-2EFFFF |
| 32 | 18000-1FFFF | 118000-11FFFF | 318000-31FFFF | 32 | | | 2E0000-2E7FFF |
| 32 | 10000-17FFF | 110000-117FFF | 310000-317FFF | 32 | | | 2D8000-2DFFFF |
| 32 | 08000-0FFFF | 108000-10FFFF | 308000-30FFFF | 32 | | | 2D0000-2D7FFF |
| 32 | 00000-07FFF | 100000-107FFF | 300000-307FFF | 32 | | | 2C8000-2CFFFF |
| 32 | | 0F8000-0FFFFF | 2F8000-2FFFFF | 32 | | | 2C0000-2C7FFF |
| 32 | | 0F0000-0F7FFF | 2F0000-2F7FFF | 32 | | | 2B8000-2BFFFF |
| 32 | | 0E8000-0EFFFF | 2E8000-2EFFFF | 32 | | | 2B0000-2B7FFF |
| 32 | | 0E0000-0E7FFF | 2E0000-2E7FFF | 32 | | | 2A8000-2AFFFF |
| 32 | | 0D8000-0DFFFF | 2D8000-2DFFFF | 32 | | | 2A0000-2A7FFF |
| 32 | | 0D0000-0D7FFF | 2D0000-2D7FFF | 32 | | | 298000-29FFFF |
| 32 | | 0C8000-0CFFFF | 2C8000-2CFFFF | 32 | | | 290000-297FFF |
| 32 | | 0C0000-0C7FFF | 2C0000-2C7FFF | 32 | | | 288000-28FFFF |
| 32 | | 0B8000-0BFFFF | 2B8000-2BFFFF | 32 | | | 280000-287FFF |
| 32 | | 0B0000-0B7FFF | 2B0000-2B7FFF | 32 | | | 278000-27FFFF |
| 32 | | 0A8000-0AFFFF | 2A8000-2AFFFF | 32 | | | 270000-277FFF |

This column continues on next page

This column continues on next page

16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing

| Top Boot | | | | Bottom Boot | | | |
|-----------|---------|---------------|---------------|-------------|-------------|---------------|---------------|
| Size (KW) | 16 Mbit | 32 Mbit | 64 Mbit | Size (KW) | 16 Mbit | 32 Mbit | 64 Mbit |
| 32 | | 0A0000-0A7FFF | 2A0000-2A7FFF | 32 | | | 268000-26FFFF |
| 32 | | 098000-09FFFF | 298000-29FFFF | 32 | | | 260000-267FFF |
| 32 | | 090000-097FFF | 290000-297FFF | 32 | | | 258000-25FFFF |
| 32 | | 088000-08FFFF | 288000-28FFFF | 32 | | | 250000-257FFF |
| 32 | | 080000-087FFF | 280000-287FFF | 32 | | | 248000-24FFFF |
| 32 | | 078000-07FFFF | 278000-27FFFF | 32 | | | 240000-247FFF |
| 32 | | 070000-077FFF | 270000-277FFF | 32 | | | 238000-23FFFF |
| 32 | | 068000-06FFFF | 268000-26FFFF | 32 | | | 230000-237FFF |
| 32 | | 060000-067FFF | 260000-267FFF | 32 | | | 228000-22FFFF |
| 32 | | 058000-05FFFF | 258000-25FFFF | 32 | | | 220000-227FFF |
| 32 | | 050000-057FFF | 250000-257FFF | 32 | | | 218000-21FFFF |
| 32 | | 048000-04FFFF | 248000-24FFFF | 32 | | | 210000-217FFF |
| 32 | | 040000-047FFF | 240000-247FFF | 32 | | | 208000-20FFFF |
| 32 | | 038000-03FFFF | 238000-23FFFF | 32 | | | 200000-207FFF |
| 32 | | 030000-037FFF | 230000-237FFF | 32 | | 1F8000-1FFFFF | 1F8000-1FFFFF |
| 32 | | 028000-02FFFF | 228000-22FFFF | 32 | | 1F0000-1F7FFF | 1F0000-1F7FFF |
| 32 | | 020000-027FFF | 220000-227FFF | 32 | | 1E8000-1EFFFF | 1E8000-1EFFFF |
| 32 | | 018000-01FFFF | 218000-21FFFF | 32 | | 1E0000-1E7FFF | 1E0000-1E7FFF |
| 32 | | 010000-017FFF | 210000-217FFF | 32 | | 1D8000-1DFFFF | 1D8000-1DFFFF |
| 32 | | 008000-00FFFF | 208000-21FFFF | 32 | | 1D0000-1D7FFF | 1D0000-1D7FFF |
| 32 | | 000000-007FFF | 200000-207FFF | 32 | | 1C8000-1CFFFF | 1C8000-1CFFFF |
| 32 | | | 1F8000-1FFFFF | 32 | | 1C0000-1C7FFF | 1C0000-1C7FFF |
| 32 | | | 1F0000-1F7FFF | 32 | | 1B8000-1BFFFF | 1B8000-1BFFFF |
| 32 | | | 1E8000-1EFFFF | 32 | | 1B0000-1B7FFF | 1B0000-1B7FFF |
| 32 | | | 1E0000-1E7FFF | 32 | | 1A8000-1AFFFF | 1A8000-1AFFFF |
| 32 | | | 1D8000-1DFFFF | 32 | | 1A0000-1A7FFF | 1A0000-1A7FFF |
| 32 | | | 1D0000-1D7FFF | 32 | | 198000-19FFFF | 198000-19FFFF |
| 32 | | | 1C8000-1CFFFF | 32 | | 190000-197FFF | 190000-197FFF |
| 32 | | | 1C0000-1C7FFF | 32 | | 188000-18FFFF | 188000-18FFFF |
| 32 | | | 1B8000-1BFFFF | 32 | | 180000-187FFF | 180000-187FFF |
| 32 | | | 1B0000-1B7FFF | 32 | | 178000-17FFFF | 178000-17FFFF |
| 32 | | | 1A8000-1AFFFF | 32 | | 170000-177FFF | 170000-177FFF |
| 32 | | | 1A0000-1A7FFF | 32 | | 168000-16FFFF | 168000-16FFFF |
| 32 | | | 198000-19FFFF | 32 | | 160000-167FFF | 160000-167FFF |
| 32 | | | 190000-197FFF | 32 | | 158000-15FFFF | 158000-15FFFF |
| 32 | | | 188000-18FFFF | 32 | | 150000-157FFF | 150000-157FFF |
| 32 | | | 180000-187FFF | 32 | | 148000-14FFFF | 148000-14FFFF |
| 32 | | | 178000-17FFFF | 32 | | 140000-147FFF | 140000-147FFF |
| 32 | | | 170000-177FFF | 32 | | 138000-13FFFF | 138000-13FFFF |
| 32 | | | 168000-16FFFF | 32 | | 130000-137FFF | 130000-137FFF |
| 32 | | | 160000-167FFF | 32 | | 128000-12FFFF | 128000-12FFFF |
| 32 | | | 158000-15FFFF | 32 | | 120000-127FFF | 120000-127FFF |
| 32 | | | 150000-157FFF | 32 | | 118000-11FFFF | 118000-11FFFF |
| 32 | | | 148000-14FFFF | 32 | | 110000-117FFF | 110000-117FFF |
| 32 | | | 140000-147FFF | 32 | | 108000-10FFFF | 108000-10FFFF |
| 32 | | | 138000-13FFFF | 32 | | 100000-107FFF | 100000-107FFF |
| 32 | | | 130000-137FFF | 32 | F8000-FFFFF | F8000-FFFFF | F8000-FFFFF |
| 32 | | | 128000-12FFFF | 32 | F0000-F7FFF | F0000-F7FFF | F0000-F7FFF |
| 32 | | | 120000-127FFF | 32 | E8000-EFFFF | E8000-EFFFF | E8000-EFFFF |
| 32 | | | 118000-11FFFF | 32 | E0000-E7FFF | E0000-E7FFF | E0000-E7FFF |
| 32 | | | 110000-117FFF | 32 | D8000-DFFFF | D8000-DFFFF | D8000-DFFFF |
| 32 | | | 108000-10FFFF | 32 | D0000-D7FFF | D0000-D7FFF | D0000-D7FFF |
| 32 | | | 100000-107FFF | 32 | C8000-CFFFF | C8000-CFFFF | C8000-CFFFF |
| 32 | | | 0F8000-0FFFFF | 32 | C0000-C7FFF | C0000-C7FFF | C0000-C7FFF |

This column continues on next page

This column continues on next page



16-Mbit, 32-Mbit, and 64-Mbit Word-Wide Memory Addressing

| Top Boot | | | | Bottom Boot | | | |
|-----------|---------|---------|---------------|-------------|-------------|-------------|-------------|
| Size (KW) | 16 Mbit | 32 Mbit | 64 Mbit | Size (KW) | 16 Mbit | 32 Mbit | 64 Mbit |
| 32 | | | 0F0000-0F7FFF | 32 | B8000-BFFFF | B8000-BFFFF | B8000-BFFFF |
| 32 | | | 0E8000-0EFFFF | 32 | B0000-B7FFF | B0000-B7FFF | B0000-B7FFF |
| 32 | | | 0E0000-0E7FFF | 32 | A8000-AFFFF | A8000-AFFFF | A8000-AFFFF |
| 32 | | | 0D8000-0DFFFF | 32 | A0000-A7FFF | A0000-A7FFF | A0000-A7FFF |
| 32 | | | 0D0000-0D7FFF | 32 | 98000-9FFFF | 98000-9FFFF | 98000-9FFFF |
| 32 | | | 0C8000-0CFFFF | 32 | 90000-97FFF | 90000-97FFF | 90000-97FFF |
| 32 | | | 0C0000-0C7FFF | 32 | 88000-8FFFF | 88000-8FFFF | 88000-8FFFF |
| 32 | | | 0B8000-0BFFFF | 32 | 80000-87FFF | 80000-87FFF | 80000-87FFF |
| 32 | | | 0B0000-0B7FFF | 32 | 78000-7FFFF | 78000-7FFFF | 78000-7FFFF |
| 32 | | | 0A8000-0AFFFF | 32 | 70000-77FFF | 70000-77FFF | 70000-77FFF |
| 32 | | | 0A0000-0A7FFF | 32 | 68000-6FFFF | 68000-6FFFF | 68000-6FFFF |
| 32 | | | 098000-09FFFF | 32 | 60000-67FFF | 60000-67FFF | 60000-67FFF |
| 32 | | | 090000-097FFF | 32 | 58000-5FFFF | 58000-5FFFF | 58000-5FFFF |
| 32 | | | 088000-08FFFF | 32 | 50000-57FFF | 50000-57FFF | 50000-57FFF |
| 32 | | | 080000-087FFF | 32 | 48000-4FFFF | 48000-4FFFF | 48000-4FFFF |
| 32 | | | 078000-077FFF | 32 | 40000-47FFF | 40000-47FFF | 40000-47FFF |
| 32 | | | 070000-077FFF | 32 | 38000-3FFFF | 38000-3FFFF | 38000-3FFFF |
| 32 | | | 068000-06FFFF | 32 | 30000-37FFF | 30000-37FFF | 30000-37FFF |
| 32 | | | 060000-067FFF | 32 | 28000-2FFFF | 28000-2FFFF | 28000-2FFFF |
| 32 | | | 058000-05FFFF | 32 | 20000-27FFF | 20000-27FFF | 20000-27FFF |
| 32 | | | 050000-057FFF | 32 | 18000-1FFFF | 18000-1FFFF | 18000-1FFFF |
| 32 | | | 048000-04FFFF | 32 | 10000-17FFF | 10000-17FFF | 10000-17FFF |
| 32 | | | 040000-047FFF | 32 | 08000-0FFFF | 08000-0FFFF | 08000-0FFFF |
| 32 | | | 038000-03FFFF | 4 | 07000-07FFF | 07000-07FFF | 07000-07FFF |
| 32 | | | 030000-037FFF | 4 | 06000-06FFF | 06000-06FFF | 06000-06FFF |
| 32 | | | 028000-02FFFF | 4 | 05000-05FFF | 05000-05FFF | 05000-05FFF |
| 32 | | | 020000-027FFF | 4 | 04000-04FFF | 04000-04FFF | 04000-04FFF |
| 32 | | | 018000-01FFFF | 4 | 03000-03FFF | 03000-03FFF | 03000-03FFF |
| 32 | | | 010000-017FFF | 4 | 02000-02FFF | 02000-02FFF | 02000-02FFF |
| 32 | | | 008000-00FFFF | 4 | 01000-01FFF | 01000-01FFF | 01000-01FFF |
| 32 | | | 000000-007FFF | 4 | 00000-00FFF | 00000-00FFF | 00000-00FFF |

Appendix F Device ID Table

| Read Configuration Addresses and Data | | | |
|---------------------------------------|-----|---------|------|
| Item | | Address | Data |
| Manufacturer Code | x16 | 00000 | 0089 |
| Device Code | | | |
| 8-Mbit x 16-T | x16 | 00001 | 88C0 |
| 8-Mbit x 16-B | x16 | 00001 | 88C1 |
| 16-Mbit x 16-T | x16 | 00001 | 88C2 |
| 16-Mbit x 16-B | x16 | 00001 | 88C3 |
| 32-Mbit x 16-T | x16 | 00001 | 88C4 |
| 32-Mbit x 16-B | x16 | 00001 | 88C5 |
| 64-Mbit x 16-T | x16 | 00001 | 88CC |
| 64-Mbit x 16-B | x16 | 00001 | 88CD |

NOTE: Other locations within the configuration address space are reserved by Intel for future use.

Appendix G Protection Register Addressing

Word-Wide Protection Register Addressing

| Word | Use | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|------|---------|----|----|----|----|----|----|----|----|
| LOCK | Both | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | Factory | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | Factory | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 2 | Factory | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 3 | Factory | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 4 | User | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 5 | User | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 6 | User | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 7 | User | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

NOTE: All address lines not specified in the above table must be 0 when accessing the Protection Register, i.e., $A_{21}A_8 = 0$.

28F800C3, 28F160C3, 28F320C3, 28F640C3



| | | |
|------------|---|----|
| 1.0 | Introduction | 1 |
| 1.1 | Product Overview..... | 2 |
| 2.0 | Product Description | 3 |
| 2.1 | Package Pinouts..... | 3 |
| 2.2 | Block Organization..... | 9 |
| 2.2.1 | Parameter Blocks..... | 9 |
| 2.2.2 | Main Blocks..... | 9 |
| 3.0 | Principles of Operation | 9 |
| 3.1 | Bus Operation | 9 |
| 3.1.1 | Read | 9 |
| 3.1.2 | Output Disable | 10 |
| 3.1.3 | Standby..... | 10 |
| 3.1.4 | Reset..... | 10 |
| 3.1.5 | Write..... | 11 |
| 3.2 | Modes of Operation | 11 |
| 3.2.1 | Read Array..... | 11 |
| 3.2.2 | Read Configuration | 12 |
| 3.2.3 | Read Status Register | 12 |
| 3.2.4 | Read Query..... | 13 |
| 3.2.5 | Program Mode | 13 |
| 3.2.6 | Erase Mode..... | 14 |
| 3.3 | Flexible Block Locking | 17 |
| 3.3.1 | Locking Operation..... | 18 |
| 3.3.2 | Unlocked State..... | 18 |
| 3.3.3 | Lock-Down State..... | 18 |
| 3.3.4 | Reading Block-Lock Status..... | 19 |
| 3.3.5 | Locking Operations during Erase Suspend | 19 |
| 3.3.6 | Status Register Error Checking | 19 |
| 3.4 | 128-Bit Protection Register | 20 |
| 3.4.1 | Reading the Protection Register..... | 20 |
| 3.4.2 | Programming the Protection Register..... | 21 |
| 3.4.3 | Locking the Protection Register | 21 |
| 3.5 | V _{PP} Program and Erase Voltages..... | 21 |
| 3.5.1 | Improved 12-Volt Production Programming..... | 21 |
| 3.5.2 | V _{PP} & V _{PPLK} for Complete Protection | 22 |
| 3.6 | Power Consumption..... | 22 |
| 3.6.1 | Active Power (Program/Erase/Read)..... | 23 |
| 3.6.2 | Automatic Power Savings (APS) | 23 |
| 3.6.3 | Standby Power..... | 23 |
| 3.6.4 | Deep Power-Down Mode..... | 23 |
| 3.7 | Power-Up/Down Operation | 23 |
| 3.7.1 | RP# Connected to System Reset | 24 |
| 3.7.2 | VCC, VPP and RP# Transitions..... | 24 |
| 3.8 | Power Supply Decoupling..... | 24 |
| 4.0 | Electrical Specifications | 25 |
| 4.1 | Absolute Maximum Ratings | 25 |
| 4.2 | Operating Conditions | 26 |
| 4.3 | Capacitance | 26 |
| 4.4 | DC Characteristics | 27 |

| | | |
|------------|---|-----------|
| 4.5 | AC Characteristics—Read Operations | 31 |
| 4.6 | AC Characteristics—Write Operations | 36 |
| 4.7 | Erase and Program Timings | 40 |
| 4.8 | Reset Operations | 42 |
| 5.0 | Ordering Information | 43 |
| 6.0 | Additional Information | 45 |
| A | WSM Current/Next States, Sheet 1 of 2 | 46 |
| B | Program/Erase Flowcharts | 48 |
| C | Common Flash Interface Query Structure | 54 |
| D | Architecture Block Diagram | 61 |
| E | Word-Wide Memory Map Diagrams | 62 |
| F | Device ID Table | 66 |
| G | Protection Register Addressing | 67 |