INTRODUCTION

The Signetics 2602 is a 1024-bit Random Access Read/Write Memory. It is fabricated with Signetics N-Channel Silicon Gate technology.

FEATURES

- 1024 x 1 ORGANIZATION
- COMPLETELY STATIC OPERATION
- +5 VOLT POWER SUPPLY ONLY
- TTL COMPATIBLE INPUTS
- THREE-STATE TTL OUTPUT
- 16-PIN DIP PACKAGE
- 200mW DISSIPATION
- N-CHANNEL SILICON GATE
- NO CLOCKS, NO REFRESHING, NO SENSING
- DOWN TO 500ns ACCESS/CYCLE TIME GUARANTEED

SUPPORT CIRCUITRY

The dominant system design characteristic for the 2602 is ease of use. This is a result of several unusual features, with fully static operation as perhaps the most important. Since the static memory cell does not depend on stored charge for its data retention, it does not need periodic refreshing. Thus, the memory does not require external circuitry to generate and control refresh cycling and refresh addresses. The on-chip support logic can also be simplified. See the block diagram in Figure 1.

BLOCK DIAGRAM

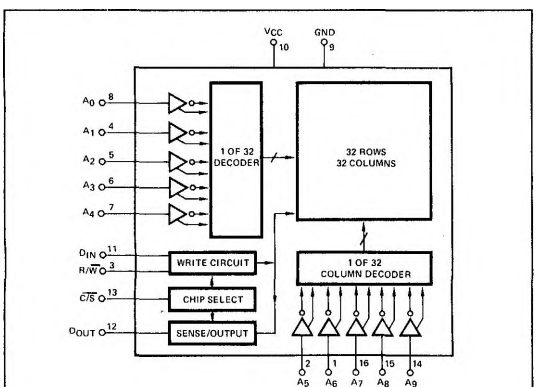

FIGURE 1

In addition to the refresh hardware costs imposed by dynamic memories, there is also a performance price to pay. Each refresh cycle ties up the memory and makes it unavailable for normal data operations. There are several interesting approaches to minimizing the performance impact of the refresh cycles, but each involves an even greater investment in support logic. Both the hardware and performance penalties of dynamic memory refreshing are eliminated by the 2602 since no refreshing of any kind is required by the device.

In the 2602 the on-chip support circuits, as well as the memory cells, are static. Thus no clocks are required for any part of the memory operation. Memory clocks for dynamic memories have proven to be very difficult to drive, distribute, and time properly so that their complete elimination saves design and debug expenses, and reduces support logic and distribution circuitry costs.

The output of the 2602 is a three-state, push-pull circuit that can drive a TTL data bus. For increased capacity several chips may be directly wire-ORed, taking advantage of the three-state output. No sense amplifiers or chip buffers are required. The problems associated with the distribution of low level sense lines and with coupled sense noise are eliminated. Figure 2 shows the output buffer circuit.

With 5 pF of typical input capacitance on any signal input and no pull-up resistors required to achieve a reliable high-level input voltage, any simple TTL logic can be used to drive arrays of the 2602 memory devices. With no high voltage, high current, or low level interface signals, noise and crosstalk problems are practically non-existent.

The net result of all these features is a dramatic decrease in the external support electronics required to implement a memory system. With greatly simplified driving, no clocks, no refreshing, and no sensing, the 2602 has eliminated all the major headaches associated with semiconductor memory system design. The cost of support electronics is also dramatically decreased. The result is that memory system costs per bit relative to dynamic memories are very attractive for 2602 memory systems of less than about 100K bits.

OUTPUT CIRCUITRY

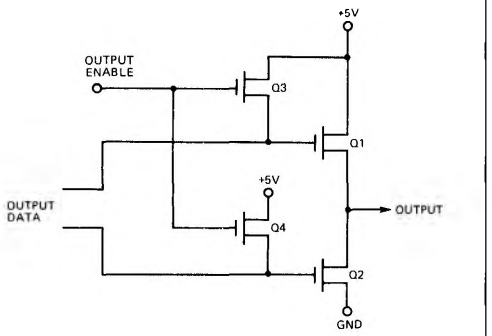

FIGURE 2

POWER

The 2602 contributes in other ways to decreased memory system costs. Only one standard supply voltage, +5V ±5%, is required. Not only are multiple supply costs eliminated, but power distribution and decoupling problems are minimized.

The low average power of less than 200mW typical and the important absence of peak currents both contribute to ease of use and lower costs. The power dissipated by the support circuits in a dynamic memory system — even a small one — can be a large percentage of the system power demands. With the 2602 static memory, the support dissipation is practically eliminated and the memory cell dissipation is very low. Power and cooling costs are, therefore, much less of a factor in the total memory system economics.

CHIP SELECT

The $\overline{\text{Chip Select}}$ signal on the 2602 performs three interrelated functions. It controls the status of the three-state output signal, it acts as the decimal address input for memories of more than 1024 words, and it enables and disables the write circuitry.

For a 1K word memory where the outputs share a data bus with other logic subsystems, the $\overline{\text{Chip Select}}$ signals can be tied together and used simply to connect or disconnect the output data from the data bus. A 2K word version of such a memory (see Figure 3) could then gate the bus connect information with the 11th address bit to form two $\overline{\text{Chip Select}}$ signals. The output data lines from the first 1K words are wire-ORed with the output data lines from the second 1K words. The two $\overline{\text{Chip Select}}$ signals will then connect the first 1K or connect the second 1K or disconnect both from the output data bus. Notice that the Read/Write lines need not be gated with the 11th address bit since an unselected chip automatically has the write circuit disabled.

READ OPERATIONS

The Read Cycle for the 2602 is very easy to execute. See the timing diagram in Figure 4. With the chip selected and in the read state, simply input an address. The data will be valid at the output after the access time has elapsed. Because there are no clocks to define the Read Cycle, it is measured as the time addresses are required to be stable. This interval is from the latest arriving address to the earliest departing address. For the same reason the access time should be measured from the latest address input.

Care should be taken to make sure that the Read/$\overline{\text{Write}}$ line is fully in the Read state before any cycle starts. Notice that one of the memory cells is being addressed at all times;

CHIP SELECT GATING

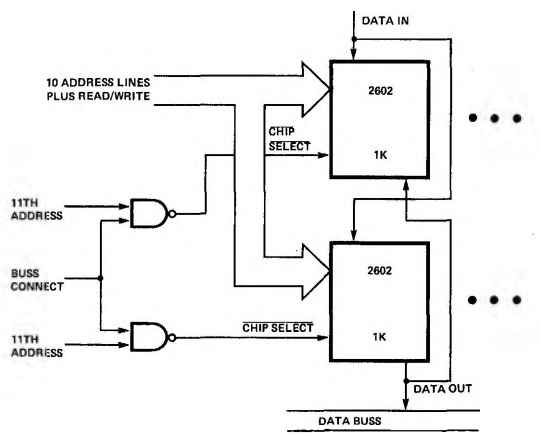

FIGURE 3

TIMING DIAGRAM

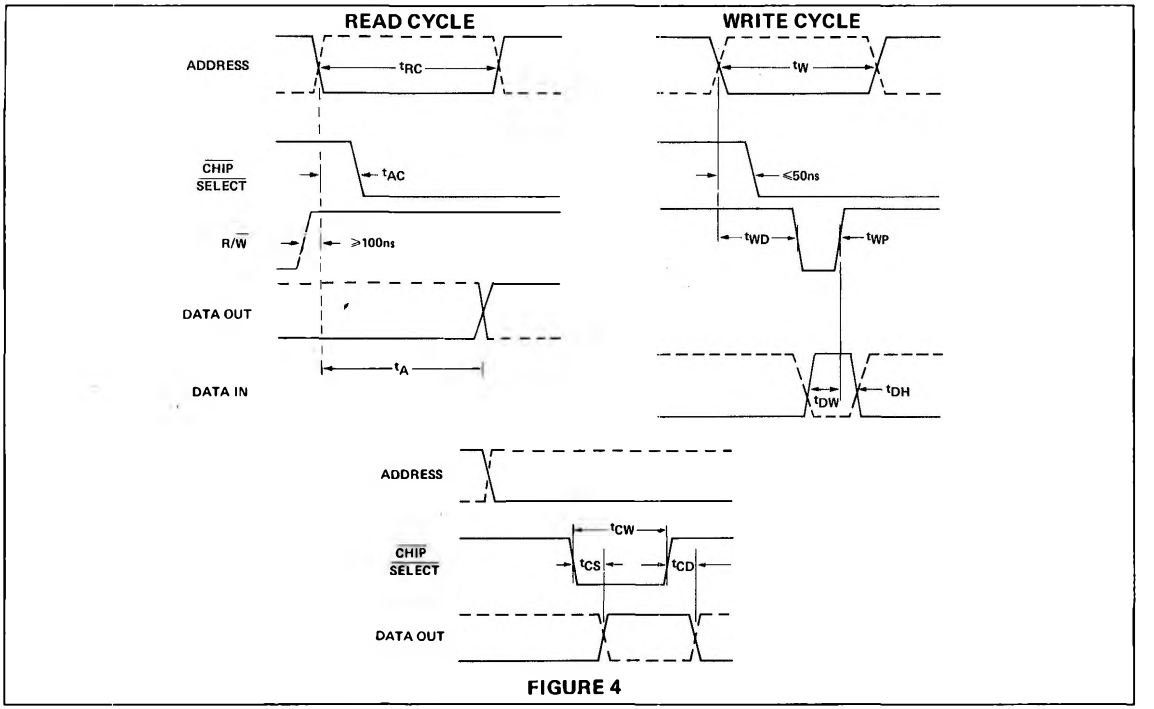

FIGURE 4

there is no quiescent state for the memory array. Thus, any time the Chip Select and Read/Write lines are both low, something will be written somewhere. The Read/Write line should be considered normally high with a negative-going write pulse allowed only under strict conditions.

The Chip Select signal may arrive as late as 200ns after the start of a Read cycle (for the 2602-1) without impacting the access time. This will often come in handy when there are extra levels of address gating involved with generating the Chip Select signal.

WRITE OPERATIONS

The write cycle is also measured by the required stable address time. Since the Chip Select signal gates the write circuitry, it must arrive earlier than in a read cycle so that the write pulse can propagate properly into the cell array. Notice that the stable addresses must overlap both the start and finish of the write pulse. It is important that the desired cell, and only the desired cell, be fully selected before the write pulse arrives and that the write pulse is fully gone before the addresses begin to change at the cell. The propagation path for the write pulse into the cell is shorter than the address path through the decoders.

For a minimum write cycle the timing of the write pulse is important. Notice in the timing diagram that t_{WD} plus t_{WP} is 400ns minimum, which leaves 100ns as the required minimum Read level before the beginning of the next cycle. A longer write cycle would allow more flexibility in the write pulse timing. The minimum write pulse width is the most critical parameter and should be maintained even if the write pulse window within the write cycle is adjusted slightly.

WAVEFORMS

The waveform picture in Figure 5 shows the 2602 in action. The test pattern being run is a simple one designed to check the general operation of every cell. The memory had previously had zeroes stored in all 1024 cells. Then a pattern of Read-Write-Read is executed at every cell location. The first Read at each cell is used to check for the previously written zero. The Write cycle then writes a one in the addressed cell and the second Read confirms that a one was in fact stored. The address then changes and the three operations are repeated on the next sequential cell.

Notice that in situations like the one pictured in Figure 5 where multiple cycles are executed at one address, there is no obvious, well-defined start of each cycle. Simple external time delays (not shown in the picture) serve to mark the transitions from cycle to cycle. The first change in the Data Out signal following the A_0 address change reflects the zero being read at the newly addressed location. During the succeeding Write cycle, the Data Out line indicates the polarity of the data being written in the cell. At the end of the Write cycle, the same cell is read again and the Data Out signal shows that a one was successfully stored. When the addresses change again, this sequence is repeated.

WAVEFORM

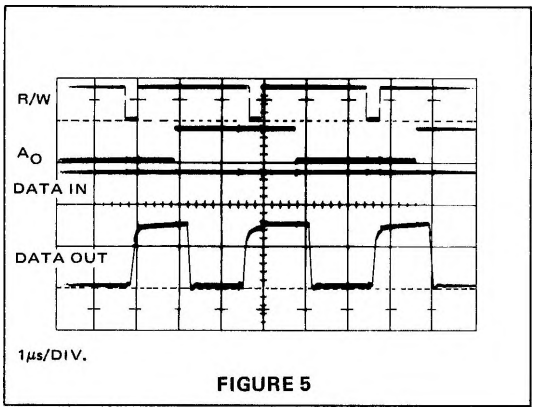

FIGURE 5

MEMORY CELL

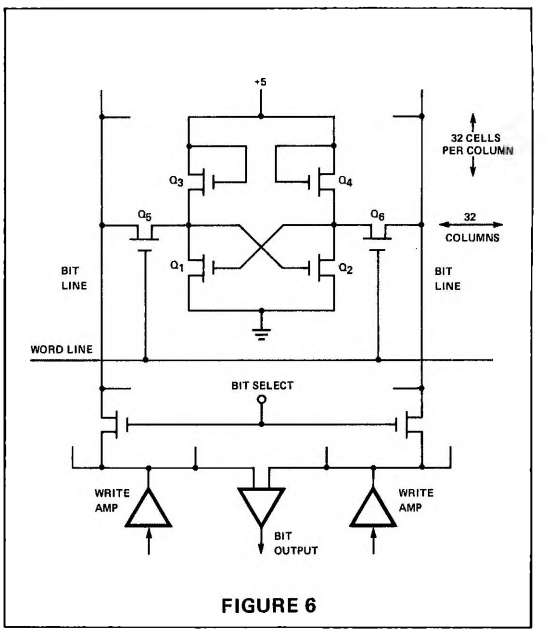

FIGURE 6

STORAGE CELL

Figure 6 is a schematic of the memory bit cell in the 2602. It is a standard six device cell configuration, using two cross-coupled devices (Q1, Q2) with active pull-ups (Q3, Q4). Q5 and Q6 are used to connect the cell to the bit lines.

The cells are arranged in a two-dimensional array of 32 by 32 for a total of 1024 cells. Address lines 0 through 4 are decoded to select 1-of-32 word lines. Each word line drives 32 cells, connecting them to 32 pairs of bit lines. Addresses 5 through 9 are decoded to select 1-of-32 bit line pairs. Thus, the 10 address lines select one cell out of 1024 for reading or writing. The bit lines are ORed together and the selected pair drive the output data amplifier.

When writing, the bit lines are driven by the write amplifiers to force the selected cell in one direction or the other. Because the bit lines are being actively driven instead of passively sensed, the write cycle can always be executed in 500ns or less even when the read cycle is longer.

MEMORY SYSTEMS

For those designers who have worked with dynamic memory systems, the dominant theme with the 2602 is the things that do not have to be done. With no clocks, no refreshing and no sensing, the designer can center his work on optimizing the TTL/MOS interfaces and the system packaging.

Because of the lack of support circuitry around the 2602, the propagation paths to and from the memory chip are much shorter than is the case with dynamic memories. This fact will help to compensate for the somewhat longer access times of the 2602, although there are large numbers of applications where the 2602 offers more than sufficient speed. The lack of support circuits makes it easy to gain performance from the static memory by interleaving. The expensive dynamic support circuitry does not have to be duplicated for a two-way interleave.

The lack of power surge currents, high voltage transitions, low level sense currents, and multiple power supplies simplifies memory system designs in several ways. One significant result is that many systems will work very well on two-sided printed circuit boards, with consequent savings in design and production costs. With less board area devoted to supporting the memory chips, the board bit density can be increased.