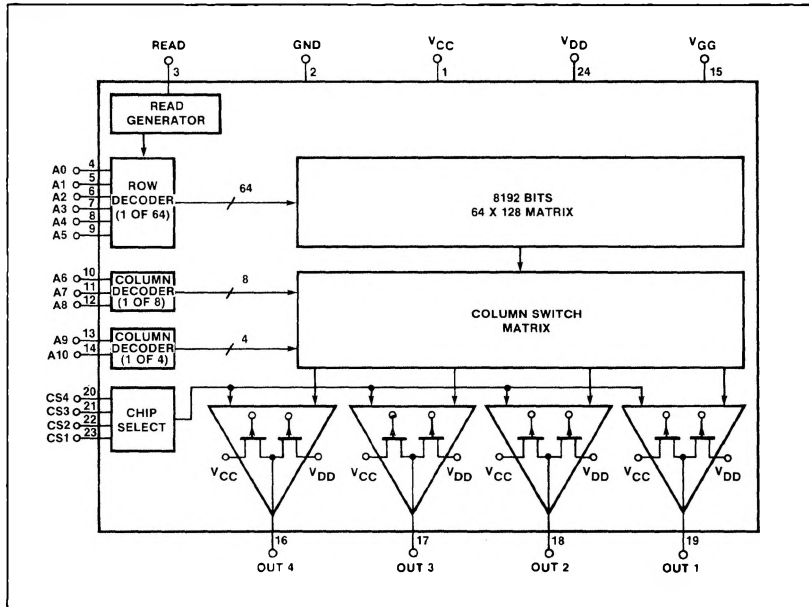


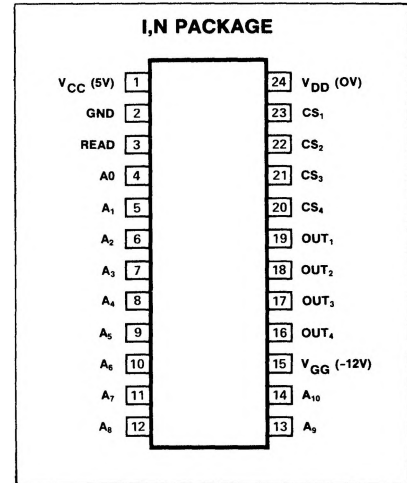
DESCRIPTION

The 2580 has a Read input which controls the entry of data from the ROM into output latches. Three-state outputs allow OR-tying for implementing larger memories. The outputs are enabled by a programmable 4-bit select code applied to 4 binary chip select terminals.

BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
T _A Operating	0 to 70	°C
T _{STG} Storage	-65 to 150	
P _D Power dissipation at 70°C ²	730	mW
Input and supply voltages with respect to V _{CC} ³	0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$
unless otherwise noted.4,5,6,7.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage ⁸ V_{IL} Low V_{IH} High		3.4		0.6	V
				5.3	
Output voltage V_{OL} Low V_{OH} High	$I_{OL} = 1.6\text{mA}$ $I_{OH} = 100\mu\text{A}$			0.5	V
I_{LI} Input load current	$V_{IN} = -5.5V$, $T_A = 25^\circ\text{C}$ $V_{OUT} = 0V$, $T_A = 25^\circ\text{C}$		10	500	nA
I_{LO} Output leakage current			10	1000	nA
Supply current ⁹ I_{CC} V_{CC} I_{GG} V_{GG}			23	35	mA
			23	35	
C_{IN} Input capacitance	$f = 1\text{MHz}$, $V_{AC} = 25\text{m p-p}$, $V_{IN} = V_{CC}$			10	pF

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$
unless otherwise specified.

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ	Max	
t_{RPW} Pulse width Read ¹⁰ t_{RPW} Read ¹¹			650	500		ns
			500	400		
t_{AD} Address time Delay ¹² t_{AH} Hold			0		50	ns
Delay time t_{A1} t_{A2}	Output	Address		625	950	ns
	Output	End of read pulse		250	350	

NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated based on a $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
- All inputs are protected against static charge.
- Parameters are valid over operating temperature range unless specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process changes and improvements.
- Typical values are at $+25^\circ\text{C}$ and typical supply voltages.
- Guaranteed input levels are stated for worst case conditions including a $\pm 5\%$ variation in V_{CC} and a temperature variation of 0°C to 70°C . Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85$ and $V_{IL} = V_{CC} - 4.15V$.
- Outputs open, $t_{RPW} = 500\text{ns}$, $t_{RPW} = 500\text{ns}$.
- During t_{RPW} addresses are decoded and sent to the memory matrix, and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (falling edge) of the read pulse. After t_{A2} , data appears at the output terminals.
- During t_{RPW} data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
- Addresses must be stable within 50ns after the read line rises and must remain stable until the read line falls.

TIMING DIAGRAM

