ADVANCE SPECIFICATION

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The 2530 is a high speed 4,096-bit Static Read-Only Memory available in a 512x8 organization. This device has TTL compatible inputs and outputs and requires +5V and −12V power supplies. A $\overline{\text{READ}}$ input controls the entry of data from the ROM into output latches. Three-state outputs allow OR tying for implementing larger memories. Two OUTPUT ENABLES control the eight output devices without affecting address circuitry.

FEATURES

- 512x8 ORGANIZATION
- 625ns TYPICAL ACCESS TIME
- STATIC OPERATION
- ADDRESS LATCHES
- TTL/DTL COMPATIBLE INPUTS
- TTL/DTL COMPATIBLE THREE STATE OUTPUTS
- V_{CC} = +5V, V_{GG} = −12V
- 24-PIN SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

MICRO-PROGRAMMING
CODE-CONVERSION

BIPOLAR COMPATIBILITY

All inputs of the 2530 can be driven directly by standard bipolar integrated circuits, (TTL, DTL, etc.). The data output buffers are capable of sinking a minimum of 1.6mA sufficient to drive one standard TTL load.

STANDARD TRUTH TABLES

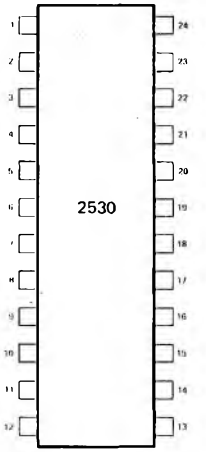
The 2530NX/CM3530 is an ASCII-EBCDIC and EBCDIC-ASCII code converter. Use this device for evaluation or for applications requiring this conversion. Other standards will be announced as they become available.

PART IDENTIFICATION

PART	OP. TEMP. RANGE	PACKAGE
2530N	0-70°C	24-Pin Silicone DIP
2530I	0-70°C	24-Pin Ceramic DIP

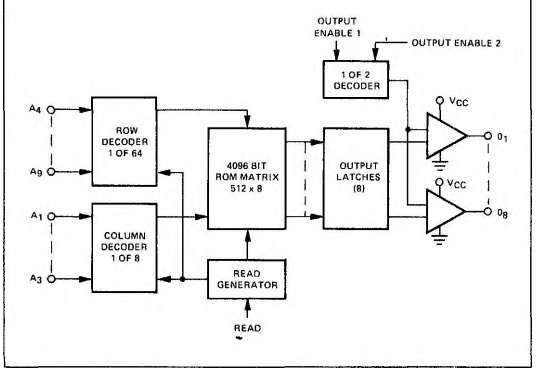
PIN CONFIGURATION (Top View)

N/I PACKAGE



1.	Output 6	24.	V_{CC}
2.	Output 7	23.	Output 5
3.	Output 8	22.	Output 4
4.	V_{DD} (Gnd)	21.	Output 3
5.	Address 1	20.	Output 2
6.	Address 2	19.	Output 1
7.	Address 3	18.	$\overline{\text{Read}}$
8.	Output Enable 1	17.	NC
9.	Output Enable 2	16.	Address 9
10.	Address 4	15.	Address 8
11.	Address 5	14.	Address 7
12.	V_{GG}	13.	Address 6

BLOCK DIAGRAM



CUSTOM TRUTH TABLES

See page 7-196.

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature	0°C to 70°C	Package Power Dissipation[2] @ 70°C	730mW
Storage Temperature	-65°C to +150°C	Input[3] and Supply Voltages with respect to V_{CC}	+0.3 to -20V

DC CHARACTERISTICS

T_A=0° to +70°C, V_{CC} = +5V; V_{GG} = −12V ±5%; unless otherwise noted. (See notes 4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = -5.5V T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{OUT} = 0V T_A = 25°C V_{CE} = V_{CC}
I_{CC}	V_{CC} Power Supply Current		30	45	mA	(8)
I_{GG}	V_{GG} Power Supply Current		30	45	mA	(8)
V_{IL}	Input Logic "0"	-5		1.05	V	
V_{IH}	Input Logic "1"	3.2		5.3	V	

AC CHARACTERISTICS

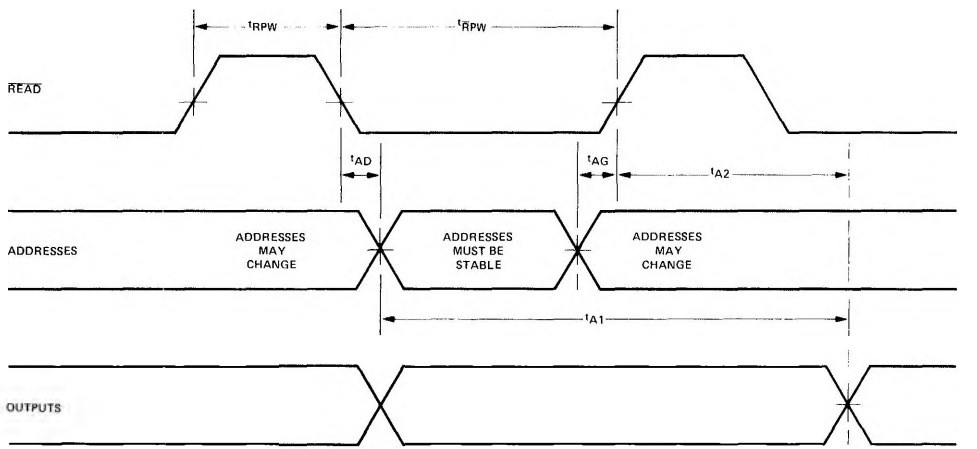
T_A = 0°C to 70°C; V_{CC} = 5V ± 5%, V_{GG} = -12V ± 5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OH}	Output Logic "zero"			0.8	V	One TTL Load
V_{OH}	Output Logic "one"	3.0			V	One TTL Load
t_{RPW}[11]	Read Pulse Width	250	200		ns	
$t_{\overline{RPW}}$[10]	$\overline{\text{Read}}$ Pulse Width	500	400		ns	
t_{AD}	Address Delay Time (12)			50	ns	
t_{AG}	Address-Read Pulse Gap (12)			50	ns	
t_{A1}	Address to Output Delay		625	700	ns	(9)
t_{A2}	End of $\overline{\text{Read}}$ Pulse to Output Delay		200	250		(9)
C_{IN}	Address Input Capacitance			10	pF	f = 1MHz, V_{AC} = 25mV p-p, V_{IN} = V_{CC}
t_{OE}	Output Enable to Output Delay		100	250	ns	f = 1MHz, V_{AC} = 25mV p-p, V_{IN} = V_{CC}

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. Outputs Open, t_{RPW} = 250ns, $t_{\overline{RPW}}$ = 500ns.
9. t_A = 0°C to +70°C
10. During t_{RPW1} data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
11. During $t_{\overline{RPW}1}$ addresses are decoded and sent to the memory matrix; and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (rising edge) of the $\overline{\text{READ}}$ pulse. After t_{A2}, data appears at the output terminals.
12. Addresses must be stable within 50ns after the $\overline{\text{READ}}$ line falls and must remain stable until at least 50ns before the $\overline{\text{READ}}$ line goes high.

TIMING DIAGRAM



Note: All times measured from 50% points, for all input waveforms tr = t_f<10nsec.