2506-T,N • 2507-T,N • 2517-T,N

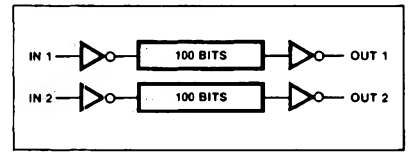
DESCRIPTION

These Signetics 2500 Series dual 100-bit Dynamic Shift Registers consist of enhancement mode p-channel MOS devices integrated on a single monolithic chip. They use 2 clock phases.

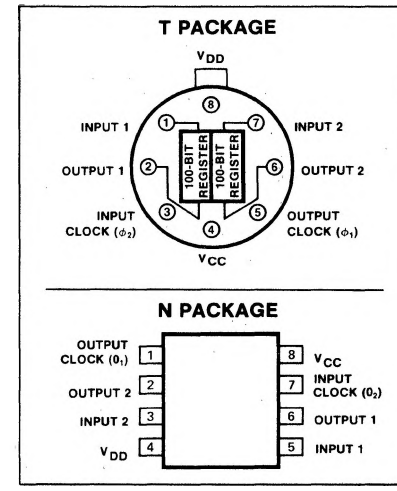
FEATURES

- **2506: Bare drain**
- **2507: 7.5K Pull down**
- **2517: 20K Pull down**

BLOCK DIAGRAM



PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
P_D	Power dissipation at T_A = 70°C[2]		mW
	T package	535	
	N package	455	
	Clock input voltages with respect to V_{CC}[3]	0.3 to -20	V
	Supply and data input voltages with respect to V_{CC}[3]	0.3 to -12	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = -5V ± 5%, V_{CC} = 5V[4], unless otherwise specified.[5,6,7,8]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[9]					V
V_{IL}	Low		-5		1.05	
V_{IH}	High		3.2		5.3	
V_{ILC}	Clock low		-12		-10	
V_{IHC}	Clock high		4		5.3	
	Output voltage[9]					V
V_{OH1}	High (driving MOS)	R_{INT} = 7.5k typ, C_L = 10pF, 2507 only	3.4	4.0		
		R_{INT} = 20k typ, 2517 only				
V_{OH2}	High (driving TTL)	R_L = 3.3k, V_{DD} = -5V, 2506 only	3.0	3.5		
I_{LI}	Load current	T_A = 25°C				nA
	Input 1	OUT 1, ϕ1, ϕ2 and V_{CC} = 5V, IN 2, OUT 2 and IN 1 = -5.5V, V_{DD} = -4.5V		10	500	
	Input 2	OUT 2, ϕ1, ϕ2 and V_{CC} = 5V, IN 1, OUT 1 and IN 2 = -5.5V, V_{DD} = -4.5V		10	500	
I_{LO}	Leakage current[10]	T_A= 25°C				nA
	Out 1	IN 1, V_{CC}, OUT 2 and ϕ2 = 5V, IN 2, V_{DD} and OUT 1 = -5.5V, ϕ1 = -5V		10	1000	
	Out 2	IN 1, OUT 1, V_{CC} and ϕ2 = 5V, IN 2, V_{DD} and OUT 2 = -5.5V, ϕ = -5V		10	1000	
I_{LC}	Clock leakage current	T_A = 25°C, V_{DD} = -4.5V, All other pins 5V				nA
	ϕ1	Vϕ1 = -12V		10	1000	
	ϕ2	Vϕ2 = -12V		10	1000	
I_{DD}	V_{DD} supply current	Outputs at logic low or high 3MHz, ϕ_1 = 150ns, ϕ_2 = 100ns		12	26	mA
	Capacitance	1MHz, 25mV p-p				pF
C_{IN}	Input (1 and 2)	V_{IN} = V_{CC}		2.5	5	
C_ϕ	Clock input (ϕ1,ϕ2)	Vϕ = V_{CC}		25	40	

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = -5V \pm 5\%$, $V_{CC} = 5V^4$, $V_{ILC} = -11V$

PARAMETER		TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
Freq.	Clock rep rate				.0006	4	3	MHz
	Pulse width			At 3MHz				ns
ϕ1PW	Clock ϕ1				150			
ϕ2PW	Clock ϕ2				100			
ϕ_d	Clock pulse delay			At 3MHz	10			ns
t_R,t_F	Clock pulse transition			At 3MHz	10		1000	ns
tw	Setup time	ϕ2	Data in		75			ns
t_{DO}	Data in overlap			$t_{R02} = t_{R01} = 10ns$	10			ns
t_{A+}	Delay time	Data out	ϕ1	$V\phi = V_{CC}$ -16V, Data out = 2.5V		90	150	ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W (T package) or 175°C/W (V package).
3. All inputs are protected against static charge.
4. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.
5. Parameters are valid over operating temperature range unless otherwise specified.
6. All voltage meuurements are referenced to ground.
7. Manufacturer reserves the right to make design and process changes and improvements.
8. Typical values are at +25°C and typical supply voltages.
9. Logic Convention: Data Lines - Positive; Clocks -Negative.
10. V_{OL} (for this bare drain device) is a function only of the driven gate characteristics together with the external pull-down resistor. (R_{PD}).

TIMING DIAGRAM