signetics

QUAD D-TYPE LATCH (WITH GATED OUTPUTS) 10133

10133F: –30 to +85°C, CERDIP

ADVANCED INFORMATION

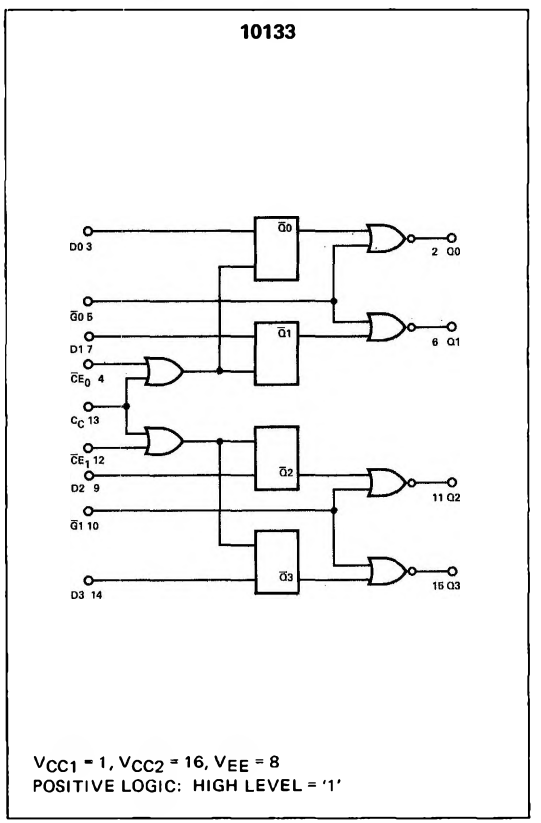
DIGITAL 10,000 SERIES ECL

DESCRIPTION

The 10133 is a high speed, low power, ECL quad latch consisting of four bistable latch circuits with D-type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is high, the outputs will follow the D inputs. Information is latched on the negative going transition of the clock.

The outputs are gated low when the output enable is high. All four latches may be clocked at one time with the common clock, or each half may be clocked separately with its clock.

LOGIC DIAGRAM



TEMPERATURE RANGE

- –30 to +85°C Operating Ambient

PACKAGE TYPE

- F: 16-Pin CERDIP

FEATURES

- FAST PROPAGATION DELAY
  - = 4.0 ns TYP CLOCK OR DATA TO OUTPUT
  - = 2.0 ns TYP ENABLE TO OUTPUT
  - = 0.7 ns TYP SETUP AND HOLD TIMES
- GATED OUTPUTS FOR BUS-ORIENTED APPLICATIONS
- HIGH DENSITY – FOUR LATCHES PLUS GATING
- LOW POWER DISSIPATION = 290 mW/PACKAGE TYP (NO LOAD)
- HIGH FANOUT CAPABILITY – CAN DRIVE FOUR 50 Ω LINES
- HIGH IMMUNITY FROM POWER SUPPLY VARIATIONS: V_{EE} = –5.2 V ±5% RECOMMENDED
- MEETS ECL 10,000 SERIES STANDARD INTERFACE SPECIFICATIONS

APPLICATIONS

- TEMPORARY STORAGE ELEMENT IN:
  - high speed central processors
  - high speed peripherals and memories
  - high speed digital communications
  - instrumentation
  - test equipment
- BUS-ORIENTED STORAGE REGISTER FOR:
  - mini-computers
  - array processors

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

$C = \overline{C_C} + C_E$

ϕ = Don't Care

NOTES:

1. For AC tests, all input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. A 50-ohm termination to ground is located in each scope input. Unused outputs are connected to a 50-ohm resistor to ground.
2. Each ECL 10,000 series device has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 fpm is maintained. Voltage levels will shift approximately 5 mV with an air flow of 200 linear fpm. Outputs are terminated through a 50-ohm resistor to –2.0 volts.

ELECTRICAL CHARACTERISTICS

(at Listed Voltages and Ambient Temperatures).

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	10133 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	–	75	–	–	mAdc	–	13	–	–	8	1,16
Input Current	I_{inH}	3	–	–	–	–	245	–	–	μAdc	3	–	–	–	8	1,16
		4	–	–	–	–	220	–	–	↓	4	–	–	–	↓	↓
		5	–	–	–	–	360	–	–		5	–	–	–		
	I_{inL}	3	–	–	0.5	–	–	–	–	μAdc	–	3	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	3,4	–	–	–	8	1,16
		2	↓	↓	↓	–	↓	↓	↓	↓	3,13	–	–	–	↓	↓
		2				–					4	–	–	–		
Logic "0" Output Voltage	V_{OL}	2	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	13	–	–	–	8	1,16
		2	↓	↓	↓	–	↓	↓	↓	↓	3,5	–	–	–	↓	↓
		2				–					13	–	–	–		
Logic "1" Threshold Voltage	V_{OHA}	2	−1.080	–	−0.980	–	−0.910	–		Vdc	3,4	–	–	5	8	1,16
		2	↓	–	↓	–	↓	–	↓	↓	4	–	3	–	↓	↓
		2		–		–		–			3,4	–	–	–		
		2†		–		–		–			3	–	–	–		
		2††		–		–		–			–	–	–	–		
		2††		–		–		–			–	–	–	4		
		2		–		–		–			3	–	4	–		
		2		–		–		–			3	–	13	–		
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.630	–	−1.595	Vdc	3,4	–	5	–	8	1,16
		2	–	↓	–	–	↓	–	↓	↓	4	–	–	3	↓	↓
		2	–		–	–		–			4	–	–	–		
		2†	–		–	–		–			–	–	–	–		
		2††	–		–	–		–			3	–	–	–		
		2††	–		–	–		–			3	–	–	13		
Switching Times † †† (50 Ω load)											+1.11 V		Pulse In	Pulse Out	−3.2 V	+2.0 V
Propagation Delay	$t_{3+\ 2+}$	2	–	–	–	4.0	–	–	–	ns	4	–	3	2	8	1,16
	$t_{4+\ 2+}$	2	–	–	–	4.0	–	–	–	↓	3	–	4	2	↓	↓
	$t_{5-\ 2+}$	2	–	–	–	2.0	–	–	–		–	–	5	2		
	t_{setup*}	3	–	–	–	0.7	–	–	–		–	–	3	2		
	t_{hold**}	3	–	–	–	0.7	–	–	–		–	–	3	2		
Rise Time (20% to 80%)	t_{2+}	2	–	–	–	2.0	–	–	–		4	–	3	2		
Fall Time (20% to 80%)	t_{2-}	2	–	–	–	2.0	–	–	–	↓	4	–	3	2	↓	↓

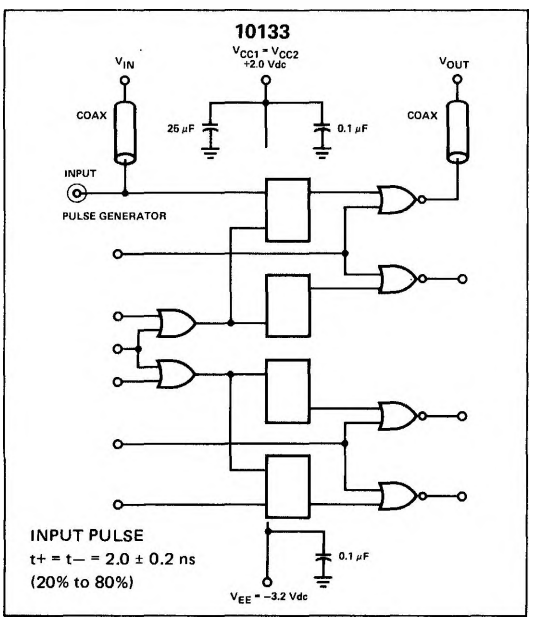
†Output level to be measured after a clock pulse has been applied to the clock input (Pin 4).

††Data input at proper high/low level while clock pulse is high so that device latches at proper high/low level for test. Levels are measured after device has latched.

*t_{setup} is minimum time before the negative transition of the clock pulse (C) that information must be present at the data input (D).

**t_{hold} is the minimum time after the negative transition of the clock pulse (C) that information must remain unchanged at the data input (D).

SWITCHING TIME TEST CIRCUIT



PROPAGATION DELAY WAVEFORMS @ 25°C