

## 100355 Low Power Quad Multiplexer/Latch

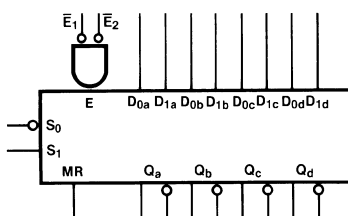
Check for Samples: [100355](#)

### FEATURES

- Greater than 40% power reduction of the 100155
- 2000V ESD protection
- Pin/function compatible with 100155
- Voltage compensated operating range =  $-4.2\text{V}$  to  $-5.7\text{V}$
- Standard Microcircuit Drawing – (SMD) 5962-9165401

### DESCRIPTION

The 100355 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ( $\bar{E}_n$ ) inputs are LOW, the data that appears at an output is controlled by the Select ( $S_n$ ) inputs, as shown in the Operating Mode table. In addition to routing data from either  $D_0$  or  $D_1$ , the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either  $D_0$  or  $D_1$  to an output. The Select inputs can be tied together for applications requiring only that data be steered from either  $D_0$  or  $D_1$ . A positive-going signal on either Enable input latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 k $\Omega$  pulldown resistors.



Pin Names	Description
$\bar{E}_1, \bar{E}_2$	Enable Inputs (Active LOW)
$\bar{S}_0, S_1$	Select Inputs
MR	Master Reset
$D_{na}-D_{nd}$	Data Inputs
$Q_a-Q_d$	Data Outputs
$\bar{Q}_a-\bar{Q}_d$	Complementary Data Outputs



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Connection Diagrams

Figure 1. 24-Pin DIP

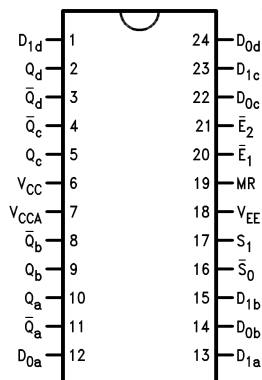
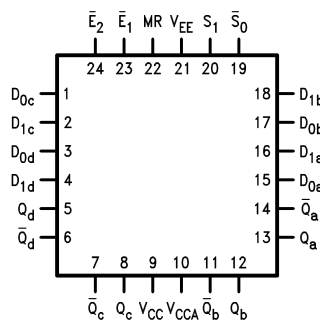
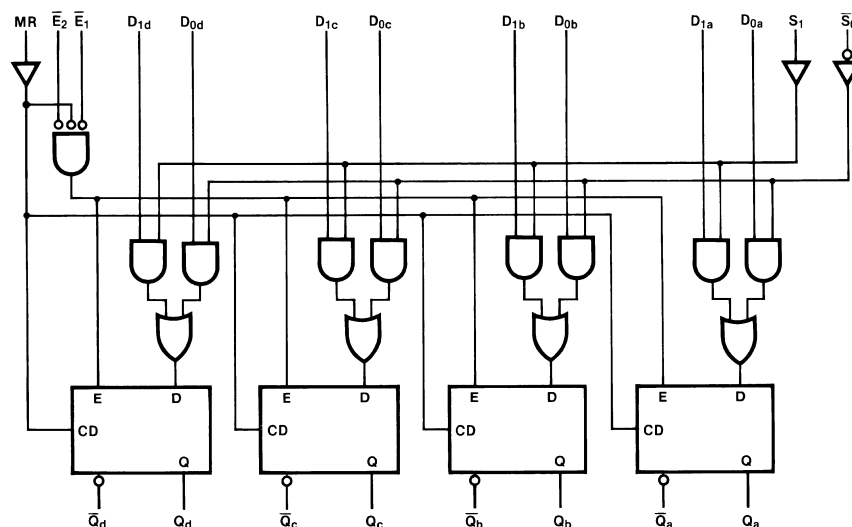


Figure 2. 24-Pin Quad Cerpak



Logic Diagram



## Operating Mode Table

Controls				Outputs
$\bar{E}_1$	$\bar{E}_2$	$S_1$	$\bar{S}_0$	$Q_n$
H	X	X	X	Latched <sup>(1)</sup>
X	H	X	X	Latched <sup>(1)</sup>
L	L	L	L	$D_{0x}$
L	L	H	L	$D_{0x} + D_{1x}$
L	L	L	H	L
L	L	H	H	$D_{1x}$

(1) Stores data present before  $\bar{E}$  went HIGH

## Truth Table

Inputs							Outputs	
MR	$\bar{E}_1$	$\bar{E}_2$	$S_1$	$\bar{S}_0$	$D_{1x}$	$D_{0x}$	$\bar{Q}_x$	$Q_x$
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched <sup>(1)</sup>	
L	X	H	X	X	X	X	Latched <sup>(1)</sup>	

(1) Stores data present before  $\bar{E}$  went HIGH



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings <sup>(1)</sup>

Above which the useful life may be impaired.

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	
Ceramic	+175°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD <sup>(2)</sup>	≥2000V

(1) Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

(2) ESD testing conforms to MIL-STD-883, Method 3015.

## Recommended Operating Conditions

Case Temperature ( $T_C$ )	
Military	-55°C to +125°C
Supply Voltage ( $V_{EE}$ )	-5.7V to -4.2V

## Military Version DC Electrical Characteristics

 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^{\circ}C$  to  $+125^{\circ}C$ 

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions		Notes	
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^{\circ}C$ to $+125^{\circ}C$				
		-1085	-870	mV	$-55^{\circ}C$	$V_{IN} = V_{IH (Max)}$	Loading with		
(1)(2)(3) $V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^{\circ}C$ to $+125^{\circ}C$	or $V_{IL (Min)}$	50 $\Omega$ to $-2.0V$		
		-1830	-1555	mV	$-55^{\circ}C$				
$V_{OHC}$	Output HIGH Voltage	-1035		mV	$0^{\circ}C$ to $+125^{\circ}C$				
		-1085		mV	$-55^{\circ}C$	$V_{IN} = V_{IH (Min)}$	Loading with	(1) (2) (3)	
$V_{OLC}$	Output LOW Voltage		-1610	mV	$0^{\circ}C$ to $+125^{\circ}C$	or $V_{IL (Max)}$	50 $\Omega$ to $-2.0V$		
			-1555	mV	$-55^{\circ}C$				
$V_{IH}$	Input HIGH Voltage	-1165	-870	mV	$-55^{\circ}C$ to	Guaranteed HIGH Signal		(1) (2) (3) (4)	
					$+125^{\circ}C$	for ALL Inputs			
$V_{IL}$	Input LOW Voltage	-1830	-1475	mV	$-55^{\circ}C$ to	Guaranteed LOW Signal		(1) (2) (3) (4)	
					$+125^{\circ}C$	for ALL Inputs			
$I_{IL}$	Input LOW Current	0.50		$\mu A$	$-55^{\circ}C$ to	$V_{EE} = -4.2V$		(1) (2) (3)	
					$+125^{\circ}C$	$V_{IN} = V_{IL (Min)}$			
$I_{IH}$	Input HIGH Current		220						
		$\bar{S}_0, S_1$		350	$\mu A$	$0^{\circ}C$ to $+125^{\circ}C$			
		$\bar{E}_1, \bar{E}_2$		340			$V_{EE} = -5.7V$		
		$D_{na}-D_{nd}$		430			$V_{IN} = V_{IH (Max)}$		(1) (2) (3)
		MR		320					
		$\bar{S}_0, S_1$		500	$\mu A$	$-55^{\circ}C$			
		$\bar{E}_1, \bar{E}_2$		490					
		$D_{na}-D_{nd}$		630					
MR									
$I_{EE}$	Power Supply Current	-95	-32	mA	$-55^{\circ}C$ to $+125^{\circ}C$	Inputs Open		(1) (2) (3)	

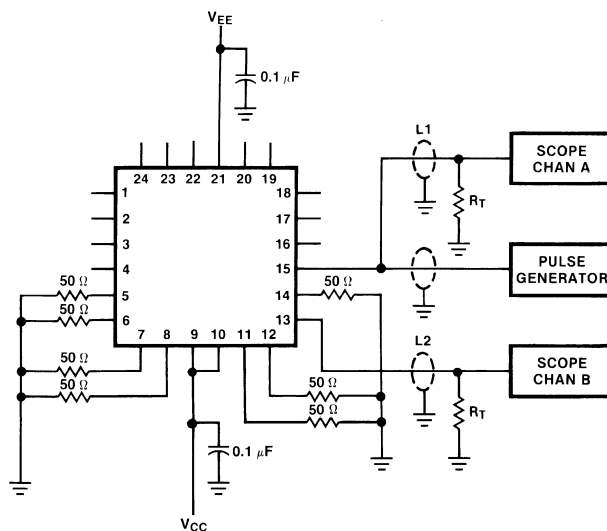
- (1) F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^{\circ}C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
- (2) Screen tested 100% on each device at  $-55^{\circ}C$ ,  $+25^{\circ}C$ , and  $+125^{\circ}C$  Temp., Subgroups 1, 2, 3, 7, and 8.
- (3) Sample tested (Method 5005, Table 1) on each Mfg. lot at  $+25^{\circ}$ ,  $+125^{\circ}C$ , and  $-55^{\circ}C$  Temp., Subgroups 1, 2, 3, 7, and 8.
- (4) Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

**Military Version  
AC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ 

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$	Propagation Delay									
$t_{PHL}$	$D_{na}-D_{nd}$ to Output (Transparent Mode)	0.40	2.30	0.50	2.20	0.50	2.60	ns		
$t_{PLH}$	Propagation Delay								(1) Figure 3	
<sup>(2)(3)(4)</sup> $t_{PHL}$	$\bar{S}_0, S_1$ to Output (Transparent Mode)	0.60	3.00	0.80	2.70	0.80	3.20	ns		
$t_{PLH}$	Propagation Delay	0.50	2.60	0.60	2.30	0.70	2.70	ns		
$t_{PHL}$	$\bar{E}_1, \bar{E}_2$ to Output									
$t_{PLH}$	Propagation Delay	0.60	2.80	0.70	2.60	0.70	2.90	ns	(1) Figure 4	(2) (3) (4)
$t_{PHL}$	MR to Output									
$t_{TLH}$	Transition Time	0.40	1.90	0.40	1.90	0.40	1.90	ns	(1) Figure 3	(5)
$t_{THL}$	20% to 80%, 80% to 20%									
$t_S$	Setup Time									
	$D_{na}-D_{nd}$	0.90		0.90		0.90		ns	(6)	(5)
	$\bar{S}_0, S_1$	2.40		2.40		2.40				
	MR (Release Time)	1.50		1.50		1.50			Figure 4	
$t_H$	Hold Time									
	$D_{na}-D_{nd}$	0.40		0.40		0.40		ns	(6)	(5)
	$\bar{S}_0, S_1$	0.00		0.00		0.00				
$t_{pw} (L)$	Pulse Width LOW $\bar{E}_1, \bar{E}_2$	2.00		2.00		2.00		ns	Figure 3	(5)
$t_{pw} (H)$	Pulse Width HIGH MR	2.00		2.00		2.00		ns	Figure 4	(5)

- (1) AC Test Circuit (Using Quad Cerpak)
- (2) F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
- (3) Screen tested 100% on each device at  $+25^\circ C$ , Temperature only, Subgroup A9.
- (4) Sample tested (Method 5005, Table 1) on each Mfg. lot at  $+25^\circ$ , Subgroup A9, and at  $+125^\circ C$ , and  $-55^\circ C$  Temp., Subgroups A10 & A11.
- (5) Not tested at  $+25^\circ C$ ,  $+125^\circ C$  and  $-55^\circ C$  Temperature (design characterization data).
- (6) Data Setup and Hold Times

## Test Circuit



### Notes:

$V_{CC}$ ,  $V_{CCA} = +2V$ ,  $V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$  terminator internal to scope

Decoupling 0.1  $\mu F$  from GND to  $V_{CC}$  and  $V_{EE}$

All unused outputs are loaded with 50Ω to GND

$C_L$  = Fixture and stray capacitance  $\leq 3$  pF

Pin numbers shown are for flatpak; for DIP see logic symbol

Switching Waveforms

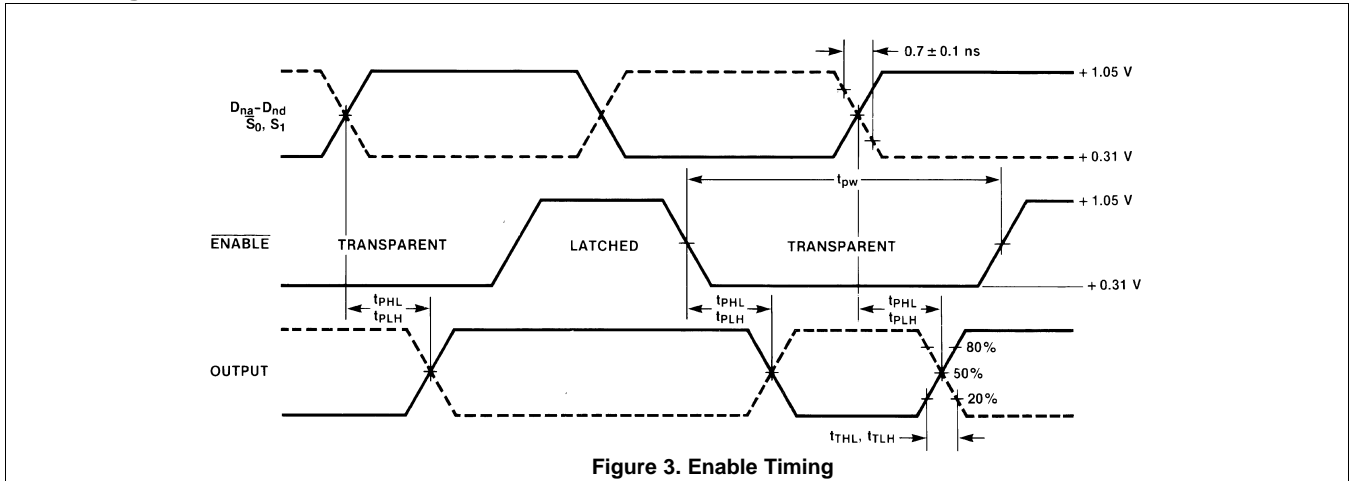


Figure 3. Enable Timing

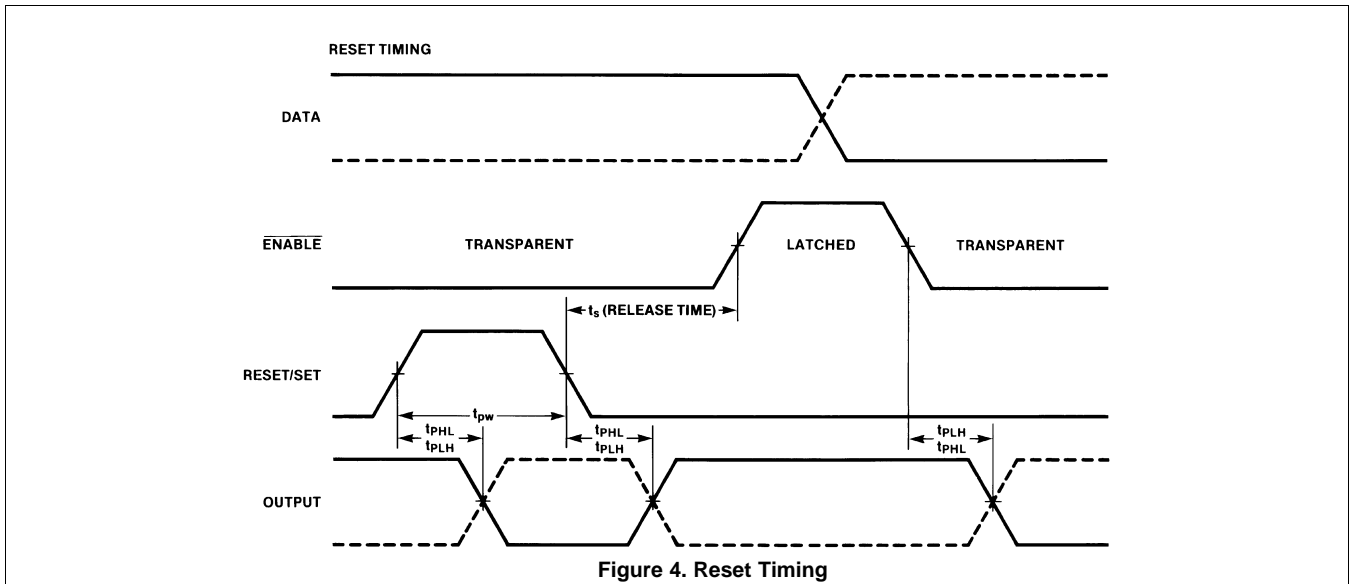
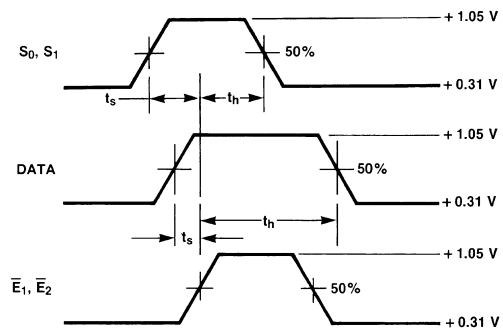


Figure 4. Reset Timing

**Notes:**

$t_s$  is the minimum time before the transition of the enable that information must be present at the data input.

$t_h$  is the minimum time after the transition of the enable that information must remain unchanged at the data input.

**Figure 5. Data Setup and Hold Times**



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